MT6356 PMIC Datasheet

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Document Revision History

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1.1	2017-06-12	Stephen Chou	Add LDO Control Power Domain Information
1.2	2017-07-04	Stephen Chou	1. Add VCAMA LDO Support 1.8V Output Voltage 2. Add Audio Output Pin AMR SPEC 3. Add Audio Negative Voltage Pin AMR SPEC

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1 Overview

1.1 Features

- Handles all 2G/3G/4G smart phone baseband power management
- Input range: 2.6V ~ 5V
- 6 buck converters and 31 LDOs optimized for specific 2G/3G/4G smart phone subsystems
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC.
- 32K RTC oscillator for system timing, 1.8 and 2.8V clock buffer output
- SPI interface
- USB Battery Charging Specification ver BC1.2 Compliance
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog reset
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- 181-pin MIFO WLCSP package

1.2 Applications

MT6356 is ideal for power management of 2G, 3G and 4G smart phones and other portable systems.

1.3 General Descriptions

MT6356 is a power management system chip optimized for 2G/3G/4G handsets and smart phones, containing 6 buck converters and 31 LDOs optimized for specific 2G/3G/4G smart phone subsystems.
Sophisticated controls are available for power-up, battery charging and the RTC alarm.

MT6356 is optimized for maximum battery life, allowing the RTC circuit to stay alive without a battery for several hours.

MT6356 adopts SPI interface and 2 SRCLKEN control pins to control buck converters, LDOs, and various drivers; it provides enhanced safety control and protocol for handshaking with BB.

MT6356 is available in a 181-pin WLCSP package. The operating temperature ranges from -30 to +85°C.

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1.4 Ordering Information

Order #	Marking	Temp. range	Package
MT6356W/A		-30 ~ +85°C	WLCSP - 181L

1.5 Top Marking Definition

MT6356W/A

YYWW: Date code
$: Random code

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1.6 Pin Assignments and Descriptions

181	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	VS1	VS1	EXT_PMIC_PG	VPA	VSYS_VPA	VSYS_VPROC	VPROC	GND_VPROC	VCORE	VSYS_VCORE	VSYS_VMODEM	VMODEM	GND_VS2	VS2	VS2	A
B	VSYS_VS1	VS1	GND_VS1	GND_VPA		VSYS_VPROC	VPROC	GND_VPROC	VCORE	VSYS_VCORE		GND_VMODEM	GND_VS2	VS2	VSYS_VS2	B
C	VSYS_VS1		GND_VS1						GND_VCORE						VSYS_VS2	C
D		PWRKEY	EXT_PMIC_EN1	RESETB	VPA_FB	VPROC_FB	GND_VPROC_FB		GND_VCORE	VCORE_FB	VMODEM_FB	GND_VMODEM_FB	VS2_FB	CHG_DP	CHG_DM	D
E	GND_SMPS	VSYS_SMPS	VMIPI	VS1_LDO1	EXT_PMIC_EN2	VCAMIO	VS1_FB	PMU_TESTMODE		GND_VCORE_FB	VSRAM_PROC	VRF12		VS2_LDO1	VDRAM	E
F	AU_V18N	FLYN	VIO18		VRF18	VCN18	D_GND	D_GND	D_GND	HOMEKEY	VSRAM_OTHERS	VS2_LDO2	VS2_LDO3	VA12	VBIF28	F
G		FLYP		AU_HPR	AU_LOLP	AU_LOLN	D_GND	D_GND	D_GND	RTC32K_1V8_1	VSRAM_GPU	VMCH	VSYS_LDO1	VCAMD		G
H	AVSS18_AUD	AVDD18_AUD		AU_HPL	AU_REFN	AU_HSN	D_GND	D_GND	D_GND	RTC32K_1V8_0		VLDO28		VCN28	VCAMA	H
J			AVDD28_AUD	HP_EINT	AVSS28_AUD	AU_HSP	FSOURCE	DVDD18_DIG		AUD_CLK_MISO	VEMC	VMC	VSYS_LDO5	VSIM2	VFE28	J
K	AU_VIN0_P		AU_VIN2_N	AU_VIN2_P	AU_MICBIAS0	ACCDET		AUD_DAT_MISO1	DVDD18_IO	AUD_SYNC_MISO	VCN33	VSYS_LDO3	VSYS_LDO4	VSIM1		K
L	AU_VIN0_N		AU_VIN1_P	AU_VIN1_N	AU_MICBIAS1		VSYS_LDO2	AUD_DAT_MOSI1	DVSS18_IO	AUD_DAT_MOSI0		VUSB	VIO28	VIBR	NC	L
M		AVSS22_XO			SRCLKEN_IN0	SRCLKEN_IN1	VAUD28	RTC32K_2V8	AUD_DAT_MISO0	NC	NC	AUD_CLK_MOSI	VSYSSNS	NC	BATSNS	M
N	XTAL1	AVSS22_XO_ISO	XO_NFC	XO_SOC	AVSS18_AUXADC		VAUX18				GND	AUD_SYNC_MOSI	CHRLDO	VCDT	ISENSE	N
P	XTAL2	AVSS22_XOBUF	XO_EXT	VXO22	AVDD18_AUXADC	CS_N	CS_P	GND	VRTC28	SPI_CLK	SPI_MOSI	SPI_CSN	UVLO_VTH	VREF	BATON	P
R	AVSS22_XOBUF	XO_CEL	XO_WCN		AUXADC_VIN		WDTRSTB_IN	GND		SPI_MISO		NC	NC	GND_VREF	NC	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 1-1. MT6356 MIFO WLCSP 181 (6.06 x 6.06mm) pin assignment

Table 1-1. MT6356 pin descriptions

Ball	Symbol	I/O	Description
A6, B6	VSYS_VPROC	PWR	Power supply of VPROC
A7, B7	VPROC	O	SW node of VPROC
A8, B8	GND_VPROC	GND	VPROC ground
D6	VPROC_FB	I	BUCK VPROC feedback pin
D7	GND_VPROC_FB	I	Remote sense on ground of VPROC
A10, B10	VSYS_VCORE	PWR	Power supply of VCORE
A9, B9	VCORE	O	SW node of VCORE
C9, D9	GND_VCORE	GND	VCORE ground

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Ball	Symbol	I/O	Description
D10	VCORE_FB	I	BUCK VCORE feedback pin
E10	GND_VCORE_FB	I	Remote sense on ground of VCORE
A11	VSYS_VMODEM	PWR	Power supply of VMODEM
A12	VMODEM	O	SW node of VMODEM
B12	GND_VMODEM	GND	VMODEM ground
D11	VMODEM_FB	I	BUCK VMODEM feedback pin
D12	GND_VMODEM_FB	I	Remote sense on ground of VMODEM
B1,C1	VSYS_VS1	PWR	Power supply of VS1
A1, A2, B2	VS1	O	SW node of VS1
B3, C3	GND_VS1	GND	VS1 ground
E7	VS1_FB	I	BUCK VS1 feedback pin
B15, C15	VSYS_VS2	PWR	Power supply of VS2
A14, A15, B14	VS2	O	SW node of VS2
A13, B13	GND_VS2	GND	VS2 ground
D13	VS2_FB	I	BUCK VS2 feedback pin
A5	VSYS_VPA	PWR	Power supply of VPA
A4	VPA	O	SW node of VPA
B4	GND_VPA	GND	VPA ground
D5	VPA_FB	I	BUCK VPA feedback pin
E2	VSYS_SMPS	PWR	Power supply of buck controller
E1	GND_SMPS	GND	GND of buck controller
J15	VFE28	O	VFE28 output voltage
H14	VCN28	O	VCN28 output voltage
H15	VCAMA	O	VCAMA output voltage
F15	VBIF28	O	VBIF28 output voltage
P4	VXO22	O	VXO22 output voltage
M7	VAUD28	O	VAUD28 output voltage
N7	VAUX18	O	VAUX18 output voltage
K11	VCN33	O	VCN33 output voltage
K14	VSIM1	O	VSIM1 output voltage
J14	VSIM2	O	VSIM2 output voltage
H12	VLDO28	O	VLDO28 output voltage
L13	VIO28	O	VIO28 output voltage
J12	VMC	O	VMC output voltage
G12	VMCH	O	VMCH output voltage
J11	VEMC	O	VEMC33 output voltage
L14	VIBR	O	VIBR output voltage
L12	VUSB	O	VUSB33 output voltage
E6	VCAMIO	O	VCAMIO output voltage
F6	VCN18	O	VCN18 output voltage
F5	VRF18	O	VRF18 output voltage
F3	VIO18	O	VIO18 output voltage
E3	VMIPI	O	VMIPI output voltage
G14	VCAMD	O	VCAMD output voltage
E12	VRF12	O	VRF12 output voltage
F14	VA12	O	VA12output voltage
E11	VSRAM_PROC	O	VSRAM_PROC output voltage
F11	VSRAM_OTHERS	O	VSRAM_OTHERS output voltage
G11	VSRAM_GPU	O	VSRAM_GPU output voltage
E15	VDRAM	O	VDRAM output voltage
E4	VS1_LDO1	PWR	2V power supply of SLDO1
E14	VS2_LDO1	PWR	1.35V power supply of SLDO1

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Ball	Symbol	I/O	Description
F12	VS2_LDO2	PWR	1.35V power supply of SLDO2
F13	VS2_LDO3	PWR	1.35V power supply of SLDO3
G13	VSYS_LDO1	PWR	Power supply input of LDO group 1
L7	VSYS_LDO2	PWR	Power supply input of LDO group 2
K12	VSYS_LDO3	PWR	Power supply input of LDO group 3
K13	VSYS_LDO4	PWR	Power supply input of LDO group 4
J13	VSYS_LDO5	PWR	Power supply input of LDO group 5
F10	HOMEKEY	I	HOMEKEY button
N15	ISENSE	I	Battery Voltage measurement
M15	BATSNS	I	VSYS supply input for internal block and UVLO detection.
M13	VSYSSNS	I	VSYS supply input for internal block
P15	BATON	I	Battery NTC pin for battery and its temperature sensing
N14	VCDT	I	Fractional charger input voltage for charger detection
L15	NC	NC	NC Ball
N13	CHRLDO	O	CHRLDO output voltage
D15	CHG_DM	I	USB D- for BC1.2 standard
D14	CHG_DP	I	USB D+ for BC1.2 standard
M14	NC	NC	NC Ball
P13	UVLO_VTH	I	UVLO threshold control pin
P14	VREF	O	Bandgap reference voltage
R14	GND_VREF	GND	Ground for bandgap
P8	GND	GND	Ground
R8	GND	GND	Ground
M8	RTC32K_2V8	O	VRTC domain 32kHz clock output
P9	VRTC28	O	RTC LDO output. Supply of RTC macro where backup battery can be added.
D2	PWRKEY	I	PWRKEY button
D4	RESETB	O	System reset release signal
E8	PMU_TESTMODE	I	PMU test mode signal (tied to GND in normal operation)
D3	EXT_PMIC_EN1	O	Ext chip enable pin 1
E5	EXT_PMIC_EN2	O	Ext chip enable pin 2
A3	EXT_PMIC_PG	I	Ext chip enable PGOOD detect
R12	NC	NC	NC Ball
R13	NC	NC	NC Ball
P6	CS_N	I	Fuel gauge ADC input pin
P7	CS_P	I	Fuel gauge ADC input pin
P5	AVDD18_AUXADC	PWR	1.8V power supply of AUXADC
N5	AVSS18_AUXADC	GND	AUXADC ground
R5	AUXADC_VIN	I	AUXADC input
M12	AUD_CLK_MOSI	I	Audio control interface
L10	AUD_DAT_MOSI0	I/O	Audio control interface
L8	AUD_DAT_MOSI1	I/O	Audio control interface
N12	AUD_SYNC_MOSI	I/O	Audio control interface
J10	AUD_CLK_MISO	O	Audio control interface
M9	AUD_DAT_MISO0	I/O	Audio control interface
K8	AUD_DAT_MISO1	I/O	Audio control interface
K10	AUD_SYNC_MISO	I/O	Audio control interface
P10	SPI_CLK	I	SPI control interface
P12	SPI_CSN	I/O	SPI control interface

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Ball	Symbol	I/O	Description
R10	SPI_MISO	I/O	SPI control interface
P11	SPI_MOSI	I/O	SPI control interface
R7	WDTRSTB_IN	I	Watchdog reset from AP
M5	SRCLKEN_IN0	I	Source clock enable pin 0
M6	SRCLKEN_IN1	I	Source clock enable pin 1
J8	DVDD18_DIG	PWR	VDIG18 output voltage
K9	DVDD18_IO	PWR	Digital IO power
L9	DVSS18_IO	GND	Digital IO power GND
H10	RTC32K_1V8_0	O	VIO18 domain 32kHz clock output
G10	RTC32K_1V8_1	O	VIO18 domain 32kHz clock output
J7	FSOURCE	PWR	EFUSE power source
G4	AU_HPR	O	Earphone right channel output
H4	AU_HPL	O	Earphone left channel output
H5	AU_REFN	GND	Audio reference ground
H6	AU_HSN	O	Handset negative output
J6	AU_HSP	O	Handset positive output
G5	AU_LOLP	O	Lineout positive output
G6	AU_LOLN	O	Lineout negative output
K6	ACCDET	I	Accessory detection input
K5	AU_MICBIAS0	O	Microphone Bias 0
L5	AU_MICBIAS1	O	Microphone Bias 1
K1	AU_VIN0_P	I	Microphone channel 0 positive input
L1	AU_VIN0_N	I	Microphone channel 0 negative input
L3	AU_VIN1_P	I	Microphone channel 1 positive input
L4	AU_VIN1_N	I	Microphone channel 1 negative input
K4	AU_VIN2_P	I	Microphone channel 2 positive input
K3	AU_VIN2_N	I	Microphone channel 2 negative input
J4	HP_EINT	I	HPL detection
H2	AVDD18_AUD	PWR	1.8V power supply of Audio
H1	AVSS18_AUD	GND	Audio DL ground
G2	FLYP	O	Flying capacitor top
F2	FLYN	O	Flying capacitor bottom
F1	AU_V18N	PWR	Audio -1.8V supply
J3	AVDD28_AUD	PWR	Power supply of Audio UL
J5	AVSS28_AUD	GND	Audio UL ground
M10	NC	NC	NC Ball
M11	NC	NC	NC Ball
P2,R1	AVSS22_XOBUF	GND	Ground for XO
R3	XO_WCN	O	26MHz output to Conn. RF
R2	XO_CEL	O	26MHz output to Cell. RF
N3	XO_NFC	O	26MHz output to NFC
N4	XO_SOC	O	26MHz output to SOC
P3	XO_EXT	O	26MHz output to UFS
M2	AVSS22_XO	GND	Ground for XO
N1	XTAL1	I/O	XTAL input 1
P1	XTAL2	I/O	XTAL input 2
N2	AVSS22_XO_ISO	GND	Connect to GSUB for DCXO noise isolation
R15	NC	NC	NC ball
N11	GND	GND	Ground
F7, F8, F9, G7, G8, G9, H7, H8, H9	D_GND	GND	Ground

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2 Electrical Characteristics

2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 2-1. Absolute maximum ratings

Parameter	Conditions	Min.	Typical	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery Pin input voltage range(1)	Steady State	-0.5		6	V
Non-Battery Power Input Pin(2)	Steady state	-0.5		5.0	V
Battery Pin input voltage range(1)	Transient State(< 10ms)	-0.5		7	V
Audio Output Pin(3)	Steady state	-5.0		5.0	V
Audio Negative Voltage Pin(4)	Steady state	-5.0		0	V
ESD robustness	HBM	2,000			V
Charger input withstand				30	V

Note:

1. VSYS_XXX/Vxxx(BUCK SW Node)/BATSNS➔Battery Input Pin(AMR=-0.5V~6V)
2. Others Pin➔ Non-Battery Power Input Pin(AMR=-0.5V~5V)
3. Audio Output Pin➔AU_HPR/AU_HPL/AU_LOLP/AU_LOLN/AU_HSN/AU_HSP
4. Audio Negative Voltage Pin➔FLYN/ AU_V18N

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2.2 Thermal Characteristic

Parameter	Conditions	Min.	Typical	Max.	Unit
Thermal resistance from junction to ambient	In free air		34.40		°C/W

Note: The device is mounted on a 10-metal-layer PCB and modeled per JEDEC51-9 condition.

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2.3 Pin Voltage Range

The table below lists operation rang voltages for all MT6356 I/O pins.

Table 2-2. Pin voltage range

Ball	Symbol	Voltage range	Unit
A6, B6	VSYS_VPROC	0 ~ 5	v
A7, B7	VPROC	0 ~ 5	v
A8, B8	GND_VPROC	0	v
D6	VPROC_FB	0 ~ 5	v
D7	GND_VPROC_FB	0	v
A10, B10	VSYS_VCORE	0 ~ 5	v
A9, B9	VCORE	0 ~ 5	v
C9, D9	GND_VCORE	0	v
D10	VCORE_FB	0 ~ 5	v
E10	GND_VCORE_FB	0	v
A11	VSYS_VMODEM	0 ~ 5	v
A12	VMODEM	0 ~ 5	v
B12	GND_VMODEM	0	v
D11	VMODEM_FB	0 ~ 5	v
D12	GND_VMODEM_FB	0	v
B1,C1	VSYS_VS1	0 ~ 5	v
A1, A2 ,B2	VS1	0 ~ 5	v
B3, C3	GND_VS1	0	v
E7	VS1_FB	0 ~ 5	v
B15, C15	VSYS_VS2	0 ~ 5	v
A14, A15, B14	VS2	0 ~ 5	v
A13, B13	GND_VS2	0	v
D13	VS2_FB	0 ~ 5	v
A5	VSYS_VPA	0 ~ 5	v
A4	VPA	0 ~ 5	v
B4	GND_VPA	0	v
D5	VPA_FB	0 ~ 5	v
E2	VSYS_SMPS	0 ~ 5	v
E1	GND_SMPS	0	v
J15	VFE28	0 ~ 5	v
H14	VCN28	0 ~ 5	v
H15	VCAMA	0 ~ 5	v
F15	VBIF28	0 ~ 5	v
P4	VXO22	0 ~ 2.42	v
M7	VAUD28	0 ~ 5	v
N7	VAUX18	0~2.2	v
K11	VCN33	0 ~ 5	v
K14	VSIM1	0 ~ 5	v
J14	VSIM2	0 ~ 5	v
H12	VLDO28	0 ~ 5	v

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Ball	Symbol	Voltage range	Unit
L13	VIO28	0 ~ 5	v
J12	VMC	0 ~ 5	v
G12	VMCH	0 ~ 5	v
J11	VEMC	0 ~ 5	v
L14	VIBR	0 ~ 5	v
L12	VUSB	0 ~ 3.63	v
E6	VCAMIO	0~2.2	v
F6	VCN18	0~2.2	v
F5	VRF18	0~2.2	v
F3	VIO18	0~2.2	v
E3	VMIPI	0~2.2	v
G14	VCAMD	0~2.2	v
E12	VRF12	0~2.2	v
F14	VA12	0~2.2	v
E11	VSRAM_PROC	0~1.4	v
F11	VSRAM_OTHERS	0~1.4	v
G11	VSRAM_GPU	0~1.4	v
E15	VDRAM	0~2.2	v
E4	VS1_LDO1	0~2.2	v
E14	VS2_LDO1	0~2.2	v
F12	VS2_LDO2	0~2.2	v
F13	VS2_LDO3	0~2.2	v
G13	VSYS_LDO1	0 ~ 5	v
L7	VSYS_LDO2	0 ~ 5	v
K12	VSYS_LDO3	0 ~ 5	v
K13	VSYS_LDO4	0 ~ 5	v
J13	VSYS_LDO5	0 ~ 5	v
F10	HOMEKEY	0~5	v
N15	ISENSE	0~5	v
M15	BATSNS	0~5	v
M13	VSYSSNS	0~5	v
P15	BATON	0~2.8	v
N14	VCDT	0~2.94	v
L15	NC	0~5	v
N13	CHRLDO	0~2.94	v
D15	CHG_DM	0~3.3	v
D14	CHG_DP	0~3.3	v
M14	NC	0~5	v
P13	UVLO_VTH	0~3.3	v
P14	VREF	0~1.32	v
R14	GND_VREF	0	v
P8	GND	0	v
R8	GND	0	v
M8	RTC32K_2V8	0~2.98	v
P9	VRTC28	0~2.98	v
D2	PWRKEY	0~5	v

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Ball	Symbol	Voltage range	Unit
D4	RESETB	0~1.98	v
E8	PMU_TESTMODE	0~5	v
D3	EXT_PMIC_EN1	0~5	v
E5	EXT_PMIC_EN2	0~5	v
A3	EXT_PMIC_PG	0~5	v
R12	NC	5.5	v
R13	NC	5.5	v
P6	CS_N	-0.1~0.1	v
P7	CS_P	-0.1~0.1	v
P5	AVDD18_AUXADC	0~1.9	v
N5	AVSS18_AUXADC	0	v
R5	AUXADC_VIN	0~1.9	v
M12	AUD_CLK_MOSI	0 ~ 1.98	v
L10	AUD_DAT_MOSI0	0 ~ 1.98	v
L8	AUD_DAT_MOSI1	0 ~ 1.98	v
N12	AUD_SYNC_MOSI	0 ~ 1.98	v
J10	AUD_CLK_MISO	0 ~ 1.98	v
M9	AUD_DAT_MISO0	0 ~ 1.98	v
K8	AUD_DAT_MISO1	0 ~ 1.98	v
K10	AUD_SYNC_MISO	0 ~ 1.98	v
P10	SPI_CLK	0~1.98	v
P12	SPI_CSN	0~1.98	v
R10	SPI_MISO	0~1.98	v
P11	SPI_MOSI	0~1.98	v
R7	WDTRSTB_IN	0~1.98	v
M5	SRCLKEN_IN0	0~1.98	v
M6	SRCLKEN_IN1	0~1.98	v
J8	DVDD18_DIG	0~1.98	v
K9	DVDD18_IO	0~1.98	v
L9	DVSS18_IO	0~1.98	v
H10	RTC32K_1V8_0	0~1.98	v
G10	RTC32K_1V8_1	0~1.98	v
J7	FSOURCE	0~1.98	v
G4	AU_HPR	-1.98 ~ 1.98	v
H4	AU_HPL	-1.98 ~ 1.98	v
H5	AU_REFN	0	v
H6	AU_HSN	-1.98 ~ 1.98	v
J6	AU_HSP	-1.98 ~ 1.98	v
G5	AU_LOLP	-1.98 ~ 1.98	v
G6	AU_LOLN	-1.98 ~ 1.98	v
K6	ACCDET	0 ~ 2.94	v
K5	AU_MICBIAS0	0 ~ 2.94	v
L5	AU_MICBIAS1	0 ~ 2.94	v
K1	AU_VIN0_P	0 ~ 2.94	v
L1	AU_VIN0_N	0 ~ 2.94	v
L3	AU_VIN1_P	0 ~ 2.94	v

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Ball	Symbol	Voltage range	Unit
L4	AU_VIN1_N	0 ~ 2.94	v
K4	AU_VIN2_P	0 ~ 2.94	v
K3	AU_VIN2_N	0 ~ 2.94	v
J4	HP_EINT	0 ~ 2.94	v
H2	AVDD18_AUD	0 ~ 1.98	v
H1	AVSS18_AUD	0	v
G2	FLYP	0 ~ 1.98	v
F2	FLYN	-1.98 ~ 0	v
F1	AU_V18N	-1.98 ~ 0	v
J3	AVDD28_AUD	0 ~ 2.94	v
J5	AVSS28_AUD	0	v
M10	NC	0~5	v
M11	NC	0~5	v
P2,R1	AVSS22_XOBUF	0	v
R3	XO_WCN	0~1.98	v
R2	XO_CEL	0~1.98	v
N3	XO_NFC	0~1.21	v
N4	XO_SOC	0~1.21	v
P3	XO_EXT	0~1.21	v
M2	AVSS22_XO	0	v
N1	XTAL1	-0.2~2.2	v
P1	XTAL2	0.2~1.7	v
N2	AVSS22_XO_ISO	0	v
R15	NC	0~5	v
N11	GND	0	v
F7, F8, F9, G7, G8, G9, H7, H8, H9	D_GND	0	v

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2.4 Recommended Operating Range

Table 2-3. Operation condition

Parameter	Conditions	Min.	Typical	Max.	Unit
Ambient temperature (T_A)		-30		85	°C
Junction temperature (T_J)		-30		125	°C
Operating input voltage		3.15 (note)		5	V

Note: This minimum input voltage still needs to check the detail test conditions for each function in specification table.

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2.5 Electrical Characteristics

VBAT = 2.6V ~ 5V, minimum loads applied on all outputs, unless otherwise noted.
Typical values are at T_A = 25°C.

Table 2-4. General electrical specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Operation Ground Current					
Standby without 32K XTAL	Low-power mode		620		μA
Power down leakage current without 32K XTAL	VBAT=4.5V, Temp=25°C			95	uA
Under Voltage (UV)					
Under voltage falling threshold		2.55	2.6	2.65	V
Under voltage rising threshold (UVLO_VTHH) w/o charger	R=200K	2.95	3.0	3.05	V
Under voltage rising threshold (UVLO_VTHH) w/i charger	R=200K	2.75	2.8	2.85	V
Reset Generator					
Output high		VIO-0.4			V
Output low				0.2	V
PWRKEY/HOMEKEY					
High voltage		0.7*VBAT			V
Low voltage				0.3*VBAT	V
De-bounce time			32		ms
Control Input Voltage					
Control input high (SPI, SRCLKEN related)		0.7*VIO			V
Control input low (SPI, SRCLKEN related)				0.3*VIO	V
Thermal Shut-down					
PMIC shut-down threshold			150		°C
Shut-down release threshold			110		°C

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2.6 Regulator Output

Table 2-5. Buck specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Buck – VPROC					
Turn-on overshoot	Vout=0.9V No load			10	%
OCP(Over Current Protect)		6		7.5	A
Temperature coefficient	VBAT=3.8V I_Load=No Load	-1		+1	%
Efficiency	VBAT=4.0V, Vout=0.8V, L_DCR=30mΩ I_Load=100mA		85		%
	VBAT=4.0V, Vout=0.8V, L_DCR=30mΩ I_Load=500mA		86		%
	VBAT=4.0V, Vout=0.8V, L_DCR=30mΩ I_Load=1.0A		79		%
	VBAT=4.0V, Vout=1.025V, L_DCR=30mΩ I_Load=5A		63		%
Soft start	Vout=0.9V No load			200	us
Switching Frequency	Iout=2.5A	1.98	2.2	2.42	MHz
Output ripple voltage (PWM)	VBAT=3.8V, I_Load=0.5*Imax 20MHz measurement BW		10		mVpp
Load transient (PWM)	VBAT=3.2V/Vout=1.023V IOUT = 1.56A to 4.92A (slew rate=3.36A/us)	-6.25% +8mV		+6.25% -8mV	%
Line transient	Vbat=3.6V to 5V IOUT = 0~half load (Tr/Tf = 15us)	-6.25% +8mV		+6.25% -8mV	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 4.5V I_Load=10mA to Imax	-5.5		+5.5	mV
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.1V to 4.5V I_Load=0~10mA	-5.5		+20	mV
Output Discharge Switch On Resistance				50	Ω
Buck – VCORE					
Turn-on overshoot	Vout=0.8V No load			10	%
OCP(Over Current Protect)		6		7.5	A
Temperature coefficient	VBAT=3.8V I_Load=No Load	-1		+1	%
Efficiency	VBAT=4.0V, Vout=0.8V, L_DCR=30mΩ I_Load=100mA		85		%
	VBAT=4.0V, Vout=0.8V,		86		%

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Parameter	Conditions	Min.	Typical	Max.	Unit
	L_DCR=30mΩ I_Load=500mA				
	VBAT=4.0V, Vout=0.8V, L_DCR=30mΩ I_Load=1.0A		79		%
	VBAT=4.0V, Vout=0.8V, L_DCR=30mΩ I_Load=5A		58		%
Soft start	Vout=0.8V No load			200	us
Switching Frequency	Iout=2.5A	1.98	2.2	2.42	MHz
Output ripple voltage (PWM)	VBAT=3.8V, I_Load=0.5*Imax 20MHz measurement BW		10		mVpp
Load transient (PWM)	VBAT=3.2V/Vout=0.8V IOUT = 1.25A to 5.15A (slew rate=3.9A/2us)	-4.75		+6.25	%
Line transient	Vbat=3.6V to 5V IOUT = 0~half load (Tr/Tf = 15us)	-4.75		+6.25	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 4.5V I_Load=10mA to Imax	-12		+4	mV
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.1V to 4.5V I_Load=0~10mA	-12		+20	mV
Output Discharge Switch On Resistance				50	Ω
Buck – VMODEM					
Turn-on overshoot	Vout=0.8V I_Load=10mA			10	%
OCP(Over Current Protect)	Imax=2A	Imax*1.2		6	A
Temperature coefficient	VBAT=3.8V PWM Mode	-1		+1	%
Efficiency	VBAT=4.0V, Vout=0.8V, L_DCR=30mΩ I_Load=400mA		86.4		%
	VBAT=4.0V, Vout=0.8V, L_DCR=30mΩ I_Load=600mA		85		%
	VBAT=4.0V, Vout=0.8V, L_DCR=30mΩ I_Load=850mA		82		%
	VBAT=4.0V, Vout=0.8V, L_DCR=30mΩ I_Load=1000mA		81		%
	VBAT=4.0V, Vout=0.8V, L_DCR=30mΩ I_Load=2000mA		69		%
Soft start	Vout=0.8V No load			1500	us
Switching Frequency	Iout=1.5A	1.08	1.2	1.32	MHz

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Parameter	Conditions	Min.	Typical	Max.	Unit
Output ripple voltage (PWM)	VBAT=3.8V, I_Load=0.5*Imax 20MHz measurement BW		10		mVpp
Load transient (PWM)	VBAT=3.8V,Vo=0.8V IOUT = 50mA to 700 mA (slew rate=1us)	-5.25		+6	%
Line transient	VBAT=3.6V to 4.5V,Vo=0.8V IOUT = 1A (Tr/Tf = 15us)	-5.25		+6	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 4.5V I_Load=PWM Load	-1		+1	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.1V to 4.5V I_Load= PFM Load	-1%		1% +31.25mV	%
Output Discharge Switch On Resistance				150	Ω
Buck – VPA					
Turn-on overshoot	Vo =3.4V , Load =10mA			10	%
OCP(Over Current Protect)	Vo=3.4V		3.2		A
Temperature coefficient	VBAT=3.8V I_Load=0.5A	-1		+1	%
Efficiency	VBAT=4.0V, Vout=0.5V, L_DCR = 55mΩ I_Load=40mA		75		%
	VBAT=4.0V, Vout=1.2V, L_DCR = 55mΩ I_Load=200mA		87		%
	VBAT=4.0V, Vout=2.4V, L_DCR = 55mΩ I_Load=400mA		91		%
	VBAT=4.0V, Vout=3.4V, L_DCR = 55mΩ I_Load=650mA		94		%
	VBAT=4.0V, Vout=3.4V, L_DCR = 55mΩ I_Load=800mA		92		%
Soft start	VBAT=3.8 ILOAD=10mA Vo=0.5V		300		us
Switching Frequency	Iout=800mA , Vout=3.4V	1.8	2	2.2	MHz
Output ripple voltage	a) PFM ripple b) PWM ripple c) PWM ripple bypass mode 0.2V < VBAT-VPA < 1.0V 20MHz measurement BW		a.150 b.50 c.100		mVp-p
Load transient	VBAT=4.0V, Vout=3.4V ILOAD= 50mA <-> 800mA (slew rate=1.6us)			400	mV
Line transient	Vbat=4.5V<->3.8V Vo=1.7V IOUT = 0.2A			200	mV

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Parameter	Conditions	Min.	Typical	Max.	Unit
	(Tr/Tf = 15us, 25C)				
DC accuracy (Included Line/Load regulation@PWM)	VBAT=3.1V to 4.5V Vout=0.5~1V	-20		+40	mV
	VBAT=3.1V to 4.5V VBAT– Vout ≥ 400 mV Vout ≥ 1V	-2		+2	%
Output Discharge Switch On Resistance				600	Ω
Buck – VS1					
Turn-on overshoot	No load			10	%
OCP(Over Current Protect)		Imax*1.2		Imax*2	A
Temperature coefficient	VBAT=3.8V I_Load=0.5*Imax/1.0*Imax	-100		+100	ppm/C
Efficiency	VBAT=4.0V, Vout=2V, L_DCR=53mΩ I_Load=50mA		90		%
	VBAT=4.0V, Vout=2V, L_DCR=53mΩ I_Load=500mA		90		%
	VBAT=4.0V, Vout=2V, L_DCR=53mΩ I_Load=1 A		87		%
	VBAT=4.0V, Vout=2V L_DCR=53mΩ I_Load=3.5 A		70		%
Soft start	No load			1	ms
Switching Frequency	Iout=1A	1.8	2	2.2	MHz
Output ripple voltage (PWM)	VBAT=3.8V, I_Load=0.5*Imax 20MHz measurement BW			0.6	%
Load transient	VBAT=3.8V IOUT = 50mA <–> 400mA. (Tr/Tf=1uS) IOUT = 20mA <–> 1200mA (Tr/Tf=5us) IOUT = 2500mA <–> 3500mA (Tr/Tf=5us)	-4.0		+5.5	%
Line transient	Vbat=3.6V to 5V IOUT = 0~half load (Tr/Tf = 15us)	-4		+5.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.2 to 5.0V I_Load=transient point to Imax	-0.9		+1.5	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.2 to 5.0V I_Load=0~ transient point	-0.9		+4.1	%
Output Discharge Switch On Resistance				100	Ω
Buck – VS2					
Turn-on overshoot	No load			10	%
OCP(Over Current Protect)		Imax*1.2		Imax*2	A

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Parameter	Conditions	Min.	Typical	Max.	Unit
Temperature coefficient	VBAT=3.8V I_Load=0.5*Imax/1.0*Imax	-100		+100	ppm/C
Efficiency	VBAT=4.0V, Vout=1.35V, L_DCR=53mΩ I_Load=50mA		84		%
	VBAT=4.0V, Vout=1.35V, L_DCR=53mΩ I_Load=500mA		89		%
	VBAT=4.0 V, Vout=1.35V, L_DCR=53mΩ I_Load=1 A		83		%
	VBAT=4.0V, Vout=1.35V L_DCR=53mΩ I_Load=3.5 A		63		%
Soft start	No load			1	ms
Switching Frequency	Iout=1A	1.8	2	2.2	MHz
Output ripple voltage (PWM)	VBAT=3.8V, I_Load=0.5*Imax 20MHz measurement BW			0.6	%
Load transient	VBAT=3.8V IOUT = 50mA <–> 400mA. (Tr/Tf=1us) IOUT = 20mA <–> 1200mA (Tr/Tf=5us) IOUT = 2500mA <–> 3500mA (Tr/Tf=5us)	-4.5		+5.5	%
Line transient	Vbat=3.6V to 5V IOUT = 0~half load (Tr/Tf = 15us)	-4.5		+5.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.2 to 5.0V I_Load=transient point to Imax	-0.9		+2.5	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.2 to 5.0V I_Load=0~ transient point	-0.9		+4.1	%
Output Discharge Switch On Resistance				100	Ω

Table 2-6. LDO specifications

Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
Power source	ALDO and DLDO	VBAT voltage (controller + power input)	max{Vo+0.3 5 ; 3.15}		5	V
	SLDO1 and SLDO2	VBAT voltage (controller input)	3.15		5	V
	SLDO1	VS1=2.0V (power input)	max{Vo+0.15 ; 2*0.95}		2*1.05	V
	SLDO2	VS2=1.35V (power input)	max{Vo+0.1 ; 1.35*0.95}		1.35*1.05	V
Overall DC voltage	ALDO, DLDO and SLDO	Default voltage	-1.5		+1.5	%

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Parameter	Type	Conditions		Min.	Typ.	Max.	Unit
accuracy	Normal mode	Non default voltage		-3		+3	%
	ALDO, DLDO and SLDO Low power mode	All voltages		-4		+4	%
Load regulation	ALDO, DLDO and SLDO Normal mode	Iout = 0mA~Imax	1. Power source 2. Typical capacitor 3. TA= -40°C~+85°C	-1.5		+1.5	%
Load regulation	ALDO, DLDO and SLDO Low power mode	Iout= 0mA~5mA	1. Power source 2. Typical capacitor 3. TA= -40°C~+85°C	-4		+4	%
Load regulation	VRTC, DVDD18_DIG	Iout = 0mA~0.2*Imax	1. Power source 2. Typical capacitor 3. TA= -40°C~+85°C	-10		+10	%
Line regulation	ALDO, DLDO and SLDO	Iout = 0mA	1. Power source 2. Typical capacitor 3. 3. TA= -40°C ~+85°C	-1.5		+1.5	%
Line regulation	VRTC, DVDD18_DIG	Iout = 0mA	1. Power source 2. Typical capacitor 3. 3. TA= -40°C ~+85°C	-5		5	%
Power off voltage	ALDO, DLDO and SLDO	Iou t= 0mA	1. Power source 2. Typical capacitor 3. TA= -40°C ~+85°C		0.1		V
Load transient response	ALDO	Iout = 1mA~0.5*Imax@ Slew rate = 15mA/us	1. Power source 2. Typical capacitor 3. TA= -40°C ~+85°C	-4		+4	%
Load transient response	DLDO and SLDO	Iout = 1mA~0.5*Imax@ Slew rate = 80mA/us	1. Power source 2. Typical capacitor 3. TA= -40°C ~+85°C	-4		+4	%
Turn-on rise time	ALDO, DLDO and SLDO	Iout = 0mA	1. Power source 2. Typical capacitor 3. TA= 25°C			300	us
Turn-on overshoot	ALDO, DLDO and SLDO	Iout = 0mA	1. Power source 2. Typical capacitor 3. TA= 25°C			+10	%
Normal mode quiescent current	ALDO	Iout = 0mA	1. Power source 2. Typical capacitor 3. TA= 25°C			55	uA
Normal mode quiescent current	DLDO	Iout = 0mA	1. Power source 2. Typical capacitor 3. TA= 25°C			55	uA
Normal mode quiescent current	SLDO (Current loading ≦0.3A)	Iout = 0mA	1. Power source 2. Typical capacitor 3. TA= 25°C			100	uA
Normal mode quiescent current	SLDO (0.3A < Current loading ≦0.6A)	Iout = 0mA	1. Power source 2. Typical capacitor 3. TA= 25°C			160	uA

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Parameter	Type	Conditions		Min.	Typ.	Max.	Unit
	SLDO (Current loading > 0.6A)					220	
	VRTC and DVDD18_DIG					10	
Low power mode quiescent current	SLDO					15	
	ALDO, DLDO					10	
Power off time	ALDO, DLDO and SLDO	Iout = 0mA	1. Power source 2. Capacitor ≦ 2.2uF 3. TA= 25°C			4	ms
			1. Power source 2. Capacitor ≦ 9.4uF 3. TA= 25°C			12	ms
Output noise	ALDO	Freq = 10Hz to 80kHz	1. Power source 2. Typical capacitor 3. TA= +25°C 4. Iout = 0.2*Imax~ 0.5*Imax		90		uVrms
	DLDO and SLDO				500		uVrms
	ALDO, DLDO and SLDO	Freq = 10Hz to 10MHz			1000		uVrms
PSRR	ALDO	Freq = 217Hz to 3kHz	1. Power source 2. Typical capacitor 3. TA= +25°C 4. Iout = 0.2*Imax~0.5*Imax		65		dB
		Freq= 3kHz to 30kHz			45		dB
	DLDO and SLDO	Freq = 217Hz			40		dB
Short current	Imax≦50mA	OC	1. Power source 2. Typical capacitor 3. TA= +25°C	60		150	mA
		OCFB		10		100	mA
	60mA≦Imax≦200mA	OC		240		600	mA
		OCFB		40		400	mA
	210mA≦Imax≦300mA	OC		360		1200	mA
		OCFB		60		800	mA
	310mA≦Imax≦450mA	OC		480		1800	mA
		OCFB		80		1200	mA
	450mA≦Imax≦600mA	OC		720		1800	mA
		OCFB		120		1200	mA
	610mA≦Imax≦800mA	OC		960		2400	mA
		OCFB		160		1600	mA
	810mA≦Imax≦1200mA	OC		1440		3600	mA
		OCFB		240		2400	mA

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2.7 Audio CODEC

Table 2-7. Audio downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to audio buffer output (single-ended output, AU_HPL/R; R_{LOAD} = 32) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, Gain = +5dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<0.1% THD		23.4		mW
SNR (1)	Signal to noise ratio (A-weighted)		107		dB(A)
THD	Total Harmonic distortion (THD) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		-96 -97 -96		dB
THD+N	THD plus noise (THD+N) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		-90 -94 -93		dB
NF_{OUT}	Output noise floor (A-weighted)		4		μVrms (A)
R_{LOAD}	Output resistor load (headphone)	16	32		Ω
C_{LOAD}	Output capacitor load			250	pF
$APGR_{DL}$	Analog programmable gain range	-10		+8	dB
$APGS_{DL}$	Analog programmable gain step		1		dB
XT_{LR}	L/R channel crosstalk @1kHz		-110		dB
PSRR	Power supply rejection ratio (From AVDD18_AUD to AU_HPL/R) @ 1kHz		-96		dB
Glitch	Click-and-Pop (CnP) suppression		-80	-75	dBVpp (rms)
DC offset	Output DC offset measured at silent input			0.3	mV
DAC to audio buffer output (single-ended output, AU_HPL/R; R_{LOAD} = 16) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, Gain = +4dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<0.1% THD		36		mW
SNR (1)	Signal to noise ratio (A-weighted)		107		dB(A)
THD	Total Harmonic distortion (THD) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		-92 -95 -94		dB
THD+N	THD plus noise (THD+N) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		-90 -93 -92		dB
NF_{OUT}	Output noise floor (A-weighted)		3.9		μVrms (A)

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer
Note 2: The output voltage range of both audio and voice buffer outputs are within [AVSS18N_AUD, AVDD18_AUD]

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Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to Line-out Output (Differential Outputs, AU_LOLP/N; R_{LOAD} = 600) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, PGA_{DL} gain = +5dB, 24bit audio data					
V_{OUT}	Maximum output swing @<1% THD @PGA_{DL} gain =+5dB gain		4.7		dBV
SNR (1)	Signal to Noise Ratio (A-weighted)		109		dB(A)
THD	Total Harmonic Distortion (THD) @ PGA_{DL} gain =+5dB gain		-90		dB
THD+N	THD Plus Noise (THD+N) @P_{OUT} = 3.2mW		-90		dB
NF_{OUT}	Output Noise Floor (A-weighted)		5.12		µVrms (A)
R_{LOAD}	Output Resistor Load (headphone)		560		Ω
C_{LOAD}	Output Capacitor Load			500	pF
$APGR_{DL}$	Analog Programmable Gain Range	-10		+8	dB
$APGS_{DL}$	Analog Programmable Gain Step		1		dB
PSRR	Power Supply Rejection Ratio (from AVDD18_AUD to AU_LOLP/N) @ 1kHz		-96		dB

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer
Note 2: The output voltage range of both audio and voice buffer outputs are within [AVSS18N_AUD, AVDD18_AUD]

Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to voice buffer output (differential outputs, AU_HSP/N; R_{LOAD} = 32) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, Gain = +5dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<1% THD		88.5		mW
SNR (1)	Signal to noise ratio (A-weighted)		110		dB(A)
THD	Total Harmonic distortion (THD) @P_{OUT} = 10mW @P_{OUT} = 50mW		 -90 -90		dB
THD+N	THD plus noise (THD+N) @P_{OUT} = 10mW @P_{OUT} = 50mW		 -90 -90		dB
NF_{OUT}	Output noise floor (A-weighted)		5.127		µVrms (A)
R_{LOAD}	Output resistor load (headphone)	16	32		Ω
C_{LOAD}	Output capacitor load			250	pF
$APGR_{DL}$	Analog programmable gain range	-10		+8	dB
$APGS_{DL}$	Analog programmable gain step		1		dB
PSRR	Power supply rejection ratio (From AVDD18_AUD to AU_HSP/N) @ 1kHz		-96		dB
DAC to voice buffer output (differential outputs, AU_HSP/N; R_{LOAD} =16) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, Gain = +4dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<1% THD		129.8		mW
SNR (1)	Signal to noise ratio (A-weighted)		109		dB(A)
THD	Total harmonic distortion (THD) @P_{OUT} = 20mW @P_{OUT} = 100mW		 -90 -90		dB
THD+N	THD Plus noise (THD+N)				dB

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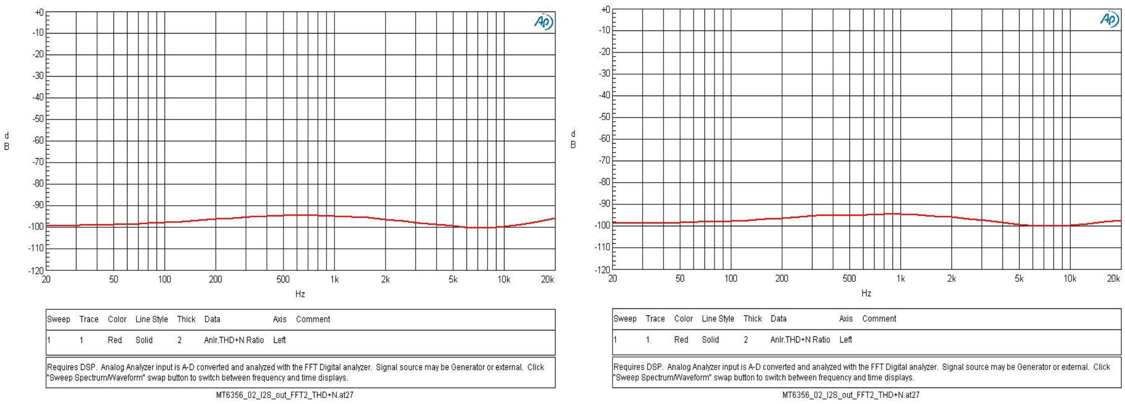
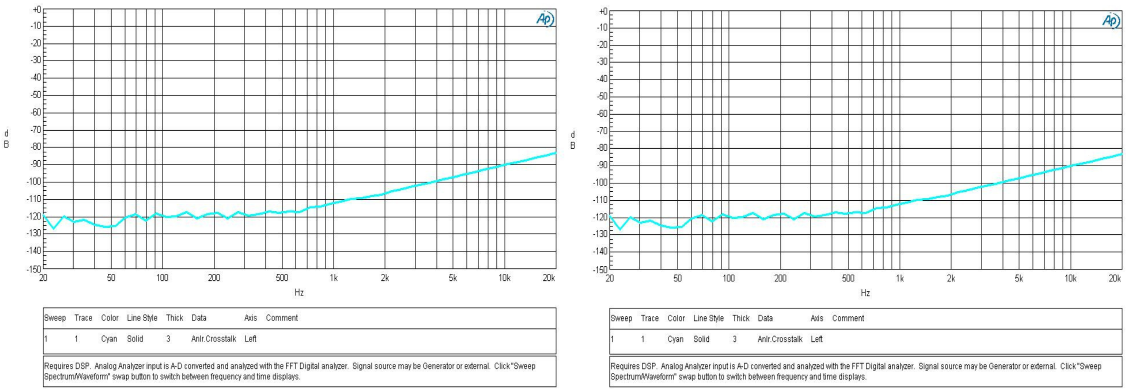
Symbol	Parameter	Min.	Typ.	Max.	Unit
	@POUT = 20mW @POUT = 100mW		-90 -90		
NFOUT	Output noise floor (A-weighted)		4.9		µVrms (A)

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer
Note 2: The output voltage range of both audio and voice buffer outputs are within [AVSS18N_AUD, AVDD18_AUD]



(a) P_{OUT}=22.5mW (b) Pout=10mW

Figure 2-1. Audio Path THD+N vs. frequency



(a) Xtalk RtoL (b) Xtalk LtoR

Figure 2-2. Audio path Xtalk vs. frequency @P_{OUT}=10mW

Table 2-8. Audio uplink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Analogue input paths to ADC (differential) DCC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 0dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		-96		dB
N_{IN}	Input-referred noise		14.3		µVrms
THD	Total Harmonic Distortion (THD) @0dBV input (-3dBFS)		-90		dB

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Symbol	Parameter	Min.	Typ.	Max.	Unit
THD+N	THD plus noise (THD+N) @0dBV input (-3dBFS)		-87		dB
	THD plus noise (THD+N) @-60dBV input (-63dBFS)		-36		dB
Analogue input paths to ADC (differential) DCC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 18dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		-85		dB
N_{IN}	Input-referred noise		6.84		μVrms
THD	Total Harmonic Distortion (THD) @-18dBV input (-3dBFS)		-90		dB
THD+N	THD plus noise (THD+N) @-18dBV input (-3dBFS)		-83		dB
	THD plus noise (THD+N) @-78dBV input (-63dBFS)		-25		dB

Symbol	Parameter	Min.	Typ.	Max.	Unit
Analogue input paths to ADC (differential) ACC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 0dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		-96		dB
N_{IN}	Input-referred noise		15.83		μVrms
THD	Total Harmonic Distortion (THD) @0dBV input (-3dBFS)		-90		dB
THD+N	THD plus noise (THD+N) @0dBV input (-3dBFS)		-88		dB
	THD plus noise (THD+N) @-60dBV input (-63dBFS)		-36		dB
Analogue Input Paths to ADC (differential) ACC mode Temp = 25deg, 1kHz sinusoid signal, FS,UL = 48kHz, PGAUL gain = 18dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		-87		dB
N_{IN}	Input-referred noise		5.37		μVrms
THD	Total Harmonic Distortion (THD) @-18dBV input (-3dBFS)		-90		dB
THD+N	THD plus noise (THD+N) @-18dBV input (-3dBFS)		-85		dB
	THD plus noise (THD+N) @-78dBV input (-63dBFS)		-27		dB

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured w/i A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer
Note 2: The input voltage range of AU_VIN0, AU_VIN1, and AU_VIN2 are within [AVDD28_AUD, AVSS28_AUD], and suggesting maximum input swing $V_{pp} \leq 1V_{rms}$ (0 dBV) @ PGA_{UL} gain = 0dB

General					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
$APGR_{UL}$	Uplink analog programmable gain range	0		24	dB
$APGS_{UL}$	Uplink analog programmable gain step		6		dB
CMRR	Common-mode rejection ratio @-18dBV, 1kHz sinusoid signal to both pins of an input configured differentially	40	75		dB
$XT_{Internal}$	ULL-to-ULR channel separation @ one input terminated with -18dBV, 1kHz sinusoid signal. Measure digital output of terminated channel	60	89		dB
XT_{DL2UL}	DL-to-UL channel separation @ 0dBV, 1kHz Rx path with RLOAD = 32	60	105		dB
PSRR	217Hz @ 200 mVpp square wave imposed on power. Measure digital output		-71		dB
	1kHz @ 200 mVpp square wave imposed on power. Measure digital output		-86		dB
	10kHz @ 200 mVpp square wave imposed on power. Measure digital output		-90		dB

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General					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
$F_{S,UL}$	Audio uplink sampling rate 8, 16, 32, and 48kHz	8		48	KHz

Digital MIC					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
DCLK	DMIC clock frequency	0.406	1.62	3.25	MHz
DTY	DMIC clock duty cycle	40		60	%
DCRT	DMIC clock rise time (MaxCL = 65p)			10	ns
DCFT	DMIC clock fall time (MaxCL = 65p)			10	ns

Table 2-9. MICBIAS specifications

Microphone Bias (MICBIAS) Temp = 25deg, 1µF capacitor on MICBIAS					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OUT}	Microphone bias voltage	1.7		2.6	V
V_{OUT} Step	Bias voltage output step size 1.7V~2.6V		0.1		V
I_{OUT}	Maximum output current (two MICBIAS loads total)			3	mA
N_{OUT}	Output integrated noise (20~20kHz A-weighted) with 1µF cap.		3.96		µVrms
PSRR	217Hz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		110		dB
	1kHz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		110		dB
	10kHz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		100		dB
$C_{LOAD,MIC}$	Output capacitor load on MICBIAS	0.1		22	µF

Table 2-10. ACCDET specifications

Accessory Detection (ACCDET)					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
-	*1: Load impedance detection range (ACCDET) by 1& 1.5kΩ (1%) MICBIAS resistors *2: The characteristics assume no other component is connected to ACCDET. *3: The key detection voltage will be normalized automatically. For different micbias settings, the same key (resistance is the same) is pressed, and the read voltage (key pressed) value will be similar.				
-	4-pole microphone detection	2k		14k	Ohm
Microphone impedance detection after 4-pole microphone plugged-in (for 3 key application)					
-	MICD_LVL[0]: Down key	400		620	Ohm
-	MICD_LVL[1]: Up key	150		320	Ohm
	MICD_LVL[2]: Hook key	0		100	Ohm

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2.8 BC1.2

Parameter	Conditions	Min.	Typical	Max.	Unit
	IPU_DP, IPU_DM	7	9.6	13	uA
	IPD_DP, IPD_DM	50	96	150	uA
	VSRC on DP, DM	500	630	700	mV

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2.9 AUXADC

Table 2-11. AUXADC specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply voltage		-	1.8	-	V
Resolution	Channel 0,1,7	-	-	15	Bits
	Others	-	-	12	Bits
Analog-input bandwidth			50K		Hz
Sample rate			100K		Hz
Offset error	Relative to full-scale	-1	-	+1	%
Gain error	Relative to full-scale	-1	-	+1	%
INL	15-bit output		2		LSB
DNL	15-bit output		2		LSB

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2.10 Fuel Gauge

Table 2-12. Fuel gauge specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
FG current characteristics	Output resolution		16		Bit
	Conversion time		1/2		s
	Over-sampling ratio	2^11		2^18	
ADC characteristics	Input voltage range	-60		60	mV
	Supply		2.8		V
	Current		40		uA
	Gain error	-2		2	%
	Accuracy		0.03		%

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2.11 BIF

Table 2-13. BIF specifications

Parameter	Description	Unit	Min.	Typ.	Max.
VIH	V input high (voltage level at input, which will be interpreted as high).	V	0.9		
VIL	V input low (voltage level at input, which will be interpreted as low.	V			0.3
VOH	V Output High.	V	1.1		2.8
VOL	When output is low, circuitry will draw BCL voltage lower than VOL voltage, measured from the output.	V	-0.3		0.1

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2.12 DCXO

Table 2-14. XO specification

Parameter	Condition	Title	Min.	Typ.	Max.	Unit
Supply current in suspend (OSC LPM)	VXO22=2.2V	$I_{xo,lpm}$		75		uA
Supply current in idle (OSC + one buffer for SOC)	VXO22=2.2V; PCB Cload<20pF	$I_{xo,idle}$		1.5		mA
Supply current in RF TRx (OSC + buffers for SOC, RF_Cell)	VXO22=2.2V; PCB Cload<20pF	$I_{xo,trx}$		4.6		mA
Extra supply current for RF_Conn	VXO22=2.2V; PCB Cload<20pF	$I_{xo,conn}$		2		mA
Extra Supply current for RF_NFC or RF_EXT	VXO22=2.2V; PCB Cload<20pF	$I_{xo,nfc}$		1		mA
Leakage current	VXO22=2.2V	$I_{xo,leak}$			1	uA
Center operating frequency	Internal resonant; with QVL crystal	F_{dcxo}		26		MHz
Duty cycle	Square wave in high driving mode		45	50	55	%
Static tuning range	XTAL1/2 differential input capacitance	C_{TR}	4.0		8.5	pF
CapID binary bits	CDAC			8		bit
Startup time, after clock request	Delta f < 1ppm.	$T_{startup}$		1	2	ms
Crystal input pins	Specific foundries			2		pin
Crystal size	CL=7~7.5pF		2016	2520	3225	

Table 2-15. Reference input buffer specification (XTAL1, buffer mode)

Parameter	Conditions	Min.	Nom.	Max.	Unit
Input Impedance – Rp	Rp || Cp @ 26MHz	3	5		kΩ
Input Impedance – Cp	Rp || Cp @ 26MHz		5	10	pF

This pin should be AC coupled when used with an external clock source.

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3 Functional Descriptions

3.1 General Descriptions

MT6356 is a fully integrated PMIC target for smart phone power provider. The following is the block diagram of MT6356 PMIC.

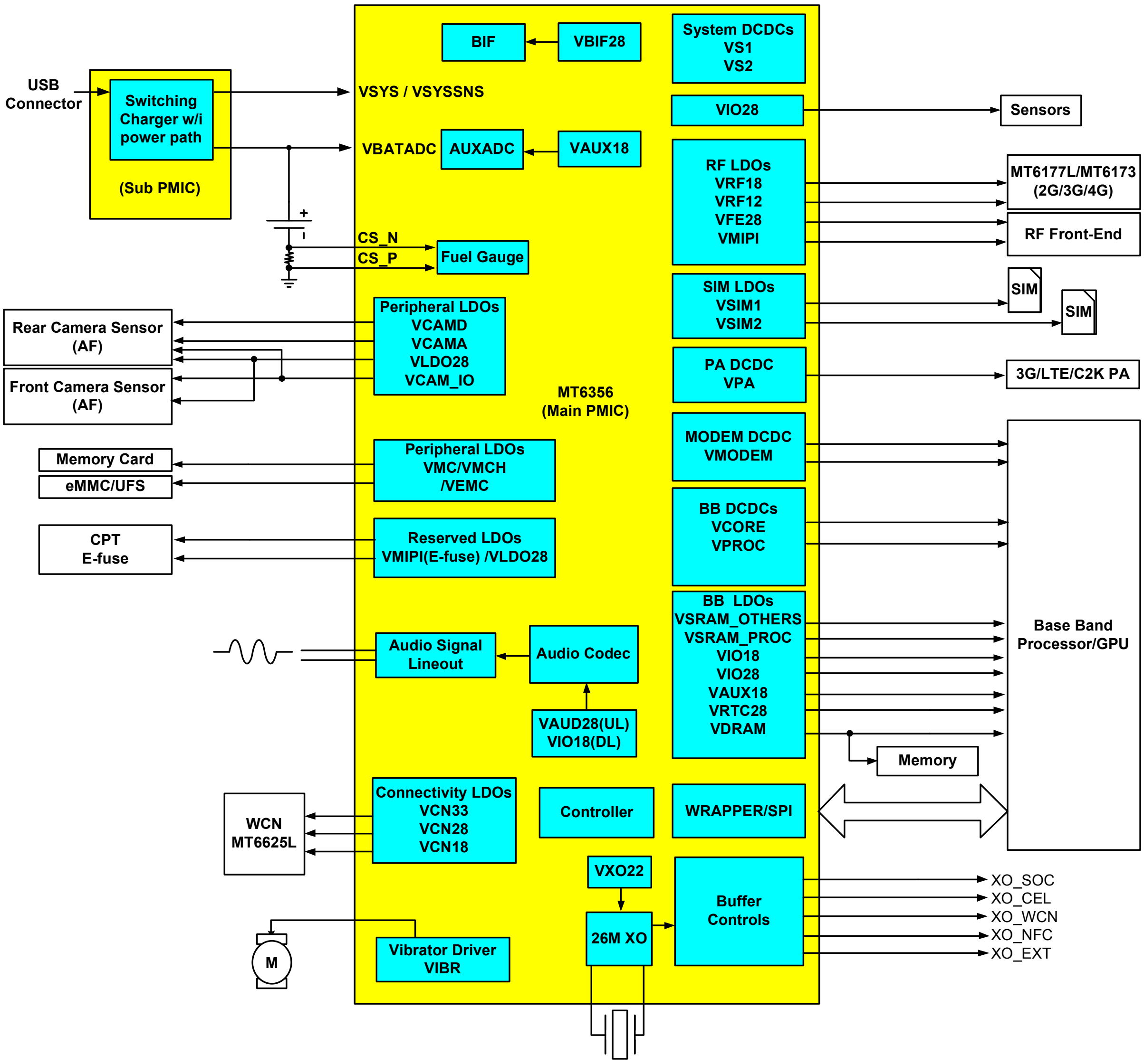

Figure 3-1. MT6356 block diagram

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3.2 PMIC Functional Blocks

MT6356 manages the power supply of baseband processor, SIM cards, camera, vibrator, etc. MT6356 includes the following analog functions for use on smart phone platforms.

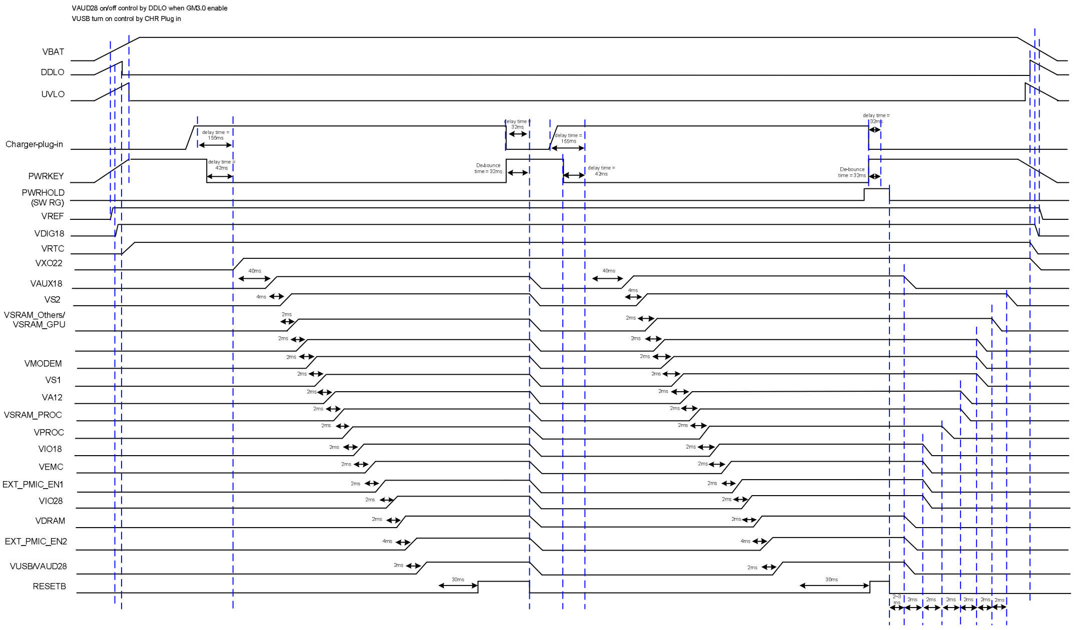
- LDO and BUCK: Provides regulated lower output voltage level from Li-Ion battery
- Vibrator driver: Provides regulated power for vibrator.
- AUXADC: 15 bits of analog to digital converter for thermal/accessory detection monitor and measurement
- Controller: Generates power-on/off sequence, system reset and exceptional handling function
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC
- Fuel gauge: Supports accurate battery capacity monitor

More detailed descriptions of each sub-block are explained in the following sections.

3.2.1 Power-On/Off Sequence

PMIC handles the power-on and power-off of the handset. If the battery voltage is neither in the UVLO state nor in the thermal condition, there are four methods to power on the handset system.

1) Pulling PWRKEY low (User presses PWRKEY.)
2) Valid charger plug-in
3) ALARM
4) SPAR



Note: Those timings are typical values; timing variation is +-20%(Charger-plug-in/out related delay timing variation is +-40%).

Figure 3-2. Power-on/off control sequence without XTAL by charger plug in or by pressing PWRKEY

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1. Pushing PWRKEY (pulling the PWRKEY pin to low level)
   Pulling PWRKEY low is a typical method to turn on the handset. The system reset ends at the moment when all default-on regulators are sequentially turned on. After that, the baseband will send the PWRHOLD signal back to PMIC for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMIC receives PWRHOLD from the baseband.

2. Valid charger plug-in (CHRIN voltage within valid range)
   The charger plug-in will also turn on the handset if the charger is valid. When PMU_CHGIN input voltage is inside valid range between CHGIN_VTHL and CHGIN_VTHH and VSYS > UVLO, the handset will also be powered on. For gauge function, VBIF28 will be turned on automatically when charger is plugged in and VSYS > DDLO.

3. RTC module generates ALARM to wake up the system.
   If the RTC module is scheduled to wake up the handset at some time, the ALARM signal will be directly sent to PMIC. In this case, ALARM becomes high at specific moment and allows PMIC power-on. This is called the RTC alarm.

4. RTC module generates SPAR to power on the system. When the sudden power drops to less than the pre-defined time period during system on and the VSYS returns to above UVLO, SPAR will be held high to allow PMIC to power on.

Under-voltage lockout (UVLO)

The UVLO state in PMIC prevents start-up if the initial voltage of the main battery is below UVLO_VTH. The judgment is done by VBATSNS. It ensures that the handset is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state and PMIC will be turned off by itself, except for VRTC28 LDO, to prevent further discharging. Once PMIC enters the UVLO state, it will draw low quiescent current. VRTC28 LDO will still be working until DDLO disables it.

Deep discharge lockout (DDLO)

PMIC will enter the deep discharge lockout (DDLO) state when the battery voltage drops below DDLO_VTHL. In this state, VRTC28 LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or even damage to the cells.

Reset

PMIC contains a reset control circuit which takes effect at both power-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter, which uses the clock from the internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

Over-temperature protection

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If the die temperature of PMIC exceeds 150°C, PMIC will automatically disable all regulators except for VRTC28. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the regulators.

3.2.2 Buck Converter and Application Reference

There are six buck converters in MT6356 to efficiently generate regulated power for graphic processor, digital core and circuits. Figure 3-1 is the block diagram. The buck converters operate with 2MHz (VS1/2 bucks and VPA)/1.2MHz (VMODEM) fixed frequency pulse width modulation (PWM) mode at moderate to heavy load currents. At light load currents, the converter automatically enters Pulse Frequency Modulation (PFM) mode to save power and improve light load efficiency. It also has a force-PWM mode option to allow the converter to remain in the PWM mode regardless of the load current, so that the noise spectrum of the converter can be minimized for certain highly-noise-sensitive handset applications. Only VPROC/VCORE bucks operate with 2.2MHz on Pseudo-PFM mode to improve mode/load transition performance. The buck converters also have an internal Over-Current Protection (OCP) circuit to limit the maximum high-side power FET current in over-load conditions. It has an internal soft start circuit to control the ramp-up rate of the output voltage during start-up. For each buck converter, there is also included auto discharging path inside switching node to confirm there won't have any remainder voltage when turned off buck. The maximum discharge resistance value are 50Ω (VPROC/VCORE) /100Ω (VS1/VS2) /150Ω (VMODEM) /600Ω (VPA) respectively.

Table 3-1. Buck converter brief specifications

BUCK name	Default voltage (V)	Vout (Volt)	Voltage step (mV)	Imax (mA)	Default on (Y/N)	Application
VPROC	0.9	0.5 ~ 1.293[2]	6.25	4,800	Y	PROCESSOR
VCORE	0.8	0.5 ~ 1.293[2]	6.25	4,800	Y	Digital core always on
VMODEM	0.8	0.5 ~ 1.15	6.25	2,000	Y	MODEM
VS1	2	1.8625~2	12.5	3,500	Y	SYS LDOs power
VS2	1.35	1.3125~1.35	12.5	3,500	Y	SYS LDOs power
VPA	0.5	0.5~3.4	50	1000 (Note)	N	3G/LTE PA

Note:

1. Due to PA application is resistance load and $R_{PA,MIN}$=4.5ohm.
   So the VPA IMAX is determined as following equation: VOUT/ $R_{PA,MIN}$ except IMAX=1000mA when VOUT≥3.4V
2. Vout range max is limited by platform application
   a. VPROC/VCORE Vout_limit=1.2V

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3.2.3 Low Dropout Regulator (LDOs) and Application Reference

Table 3-2. LDO types and brief specifications

Type	LDO name	Input power domain	Controller power domain	Default voltage	Vout (Volt)	Imax (mA)	Application
ALDO	VFE28	VSYS_LDO1	VSYS_LDO1	2.8	2.8	40mA	RFFE
ALDO	VXO22	VSYS_LDO2	VSYS_LDO2	2.24	2.24/2.375	25mA	DCXO
SLDO	VRF18	VS1_LDO1	VSYS_SMPS	1.81	1.81	450mA	RF
SLDO	VRF12	VS2_LDO1	VSYS_LDO1	1.2	1.2	210mA	RF
SLDO	VMIPI	VS1_LDO1	VSYS_SMPS	1.8	1.71/1.8/1.84	300mA	RF MIPI and EFUSE
DLDO	VCN33	VSYS_LDO3	VSYS_LDO3	3.3	3.3/3.4/3.5/3.6	800mA	WCN
ALDO	VCN28	VSYS_LDO1	VSYS_LDO1	2.8	2.8	40mA	WCN
SLDO	VCN18	VS1_LDO1	VSYS_SMPS	1.8	1.8	210mA	WCN
ALDO	VCAMA	VSYS_LDO1	VSYS_LDO1	2.8	1.8/2.5/2.8	200mA	CAMERA
SLDO	VCAMIO	VS1_LDO1	VSYS_SMPS	1.8	1.8	300mA	CAMERIO
SLDO	VCAMD	VS2_LDO3	VSYS_LDO1	1.2	1.0/1.05/1.1/1.2/1.3/1.5/1.8	600mA	CAMERD
DLDO	VLDO28	VSYS_LDO5	VSYS_LDO5	2.8	2.8/3.0	360mA	Touch panel and CAMERA_AF
SLDO	VA12	VS2_LDO1	VSYS_LDO1	1.2	1.2	300mA	AP ABB
ALDO	VAUX18	VSYS_LDO2	VSYS_LDO2	1.8	1.8	20mA	AUXADC
ALDO	VAUD28	VSYS_LDO2	VSYS_LDO2	2.8	2.8	50mA	Audio
DLDO	VIO28	VSYS_LDO4	VSYS_LDO4	2.8	2.8	200mA	IO and sensor
SLDO	VIO18	VS1_LDO1	VSYS_SMPS	1.8	1.8	1200mA	IO and eMMC
SLDO	VSRAM_PROC	VS2_LDO2	VSYS_LDO1	1.1	0.6~1.31	400mA	SRAM_PROC
SLDO	VSRAM_GPU	VS2_LDO2	VSYS_LDO1	1.0	0.6~1.31	400mA	SRAM_GPU
SLDO	VSRAM_OTHERS	VS2_LDO2	VSYS_LDO1	0.9	0.6~1.31	400mA	SRAM_OTHERS
SLDO	VDRAM	VS2_LDO1	VSYS_LDO1	1.24	1.12/1.24	1,000mA	DRAM
DLDO	VMC	VSYS_LDO5	VSYS_LDO5	3	1.86/2.9/3.0/3.3	200mA	MSDC
DLDO	VMCH	VSYS_LDO5	VSYS_LDO5	3	2.9/3.0/3.3	800mA	SD card
DLDO	VEMC	VSYS_LDO3	VSYS_LDO3	3	2.9/3.0/3.3	800mA	eMMC and UFS
DLDO	VSIM1	VSYS_LDO4	VSYS_LDO4	1.86	1.7/1.8/1.86/2.76/3.0/3.1	200mA	SIM1 card
DLDO	VSIM2	VSYS_LDO4	VSYS_LDO4	1.86	1.7/1.8/1.86/2.76/3.0/3.1	200mA	SIM2 card
DLDO	VIBR	VSYS_LDO4	VSYS_LDO4	2.8	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	200mA	Vibrator

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Type	LDO name	Input power domain	Controller power domain	Default voltage	Vout (Volt)	Imax (mA)	Application
DLDO	VUSB	VSYS_LDO3	VSYS_LDO3	3.07	3.07	60mA	USB
ALDO	VBIF28	VSYS_LDO1	VSYS_LDO1	2.8	2.8	1mA	BIF
VRTC28	VRTC28	VSYSSNS	VSYSSNS	2.8	2.8	2mA	RTC macro
VDIG18	DVDD18_DIG	VSYSSNS	VSYSSNS	1.8	1.8	10mA	PMIC digital

3.2.4 Vibrator Driver

The VIBR driver power allows up to 200mA current for ERM (Eccentric Rotating Mass) or coin type vibrator with programmable output voltage.

3.2.5 Audio CODEC and Accessory Detection

3.2.5.1 Block Descriptions

The block diagram of audio codec is illustrated below. The audio uplink path is composed of PGA and audio ADC. There are three input pairs of the uplink path to support dual-MIC, earphone-MIC, and digital MIC. The uplink front-end to PGA can be configured as ACC or DCC type. The audio downlink is composed of stereo audio DACs, stereo headphone drivers and a mono voice driver. High-fidelity audio is reproduced on headphones and clear mobile speech on earpiece is driven by voice drivers. The internal high output power loud-speaker amplifier is also embedded. The necessary MIC bias voltages and multi-key accessory detection are also provided by this completed audio codec.

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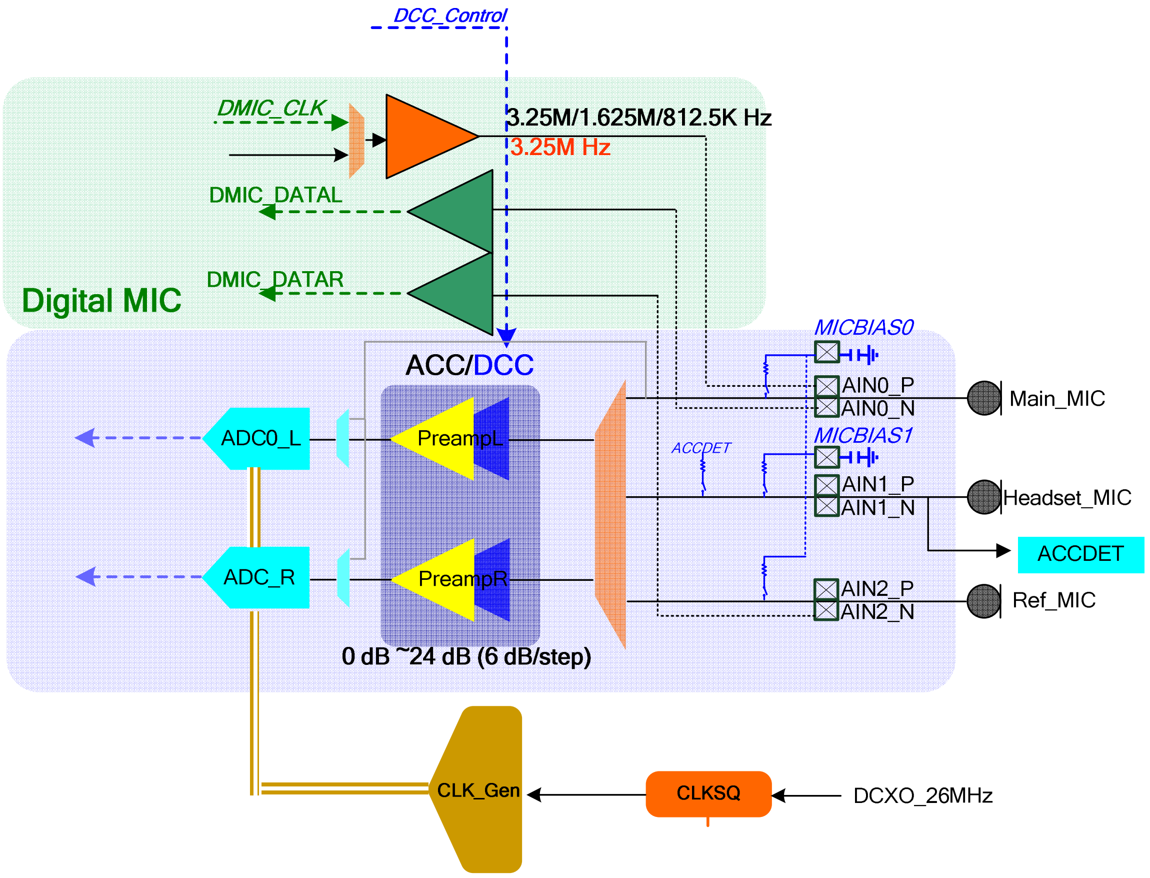

(a) Audio/speech uplink and accessory detection

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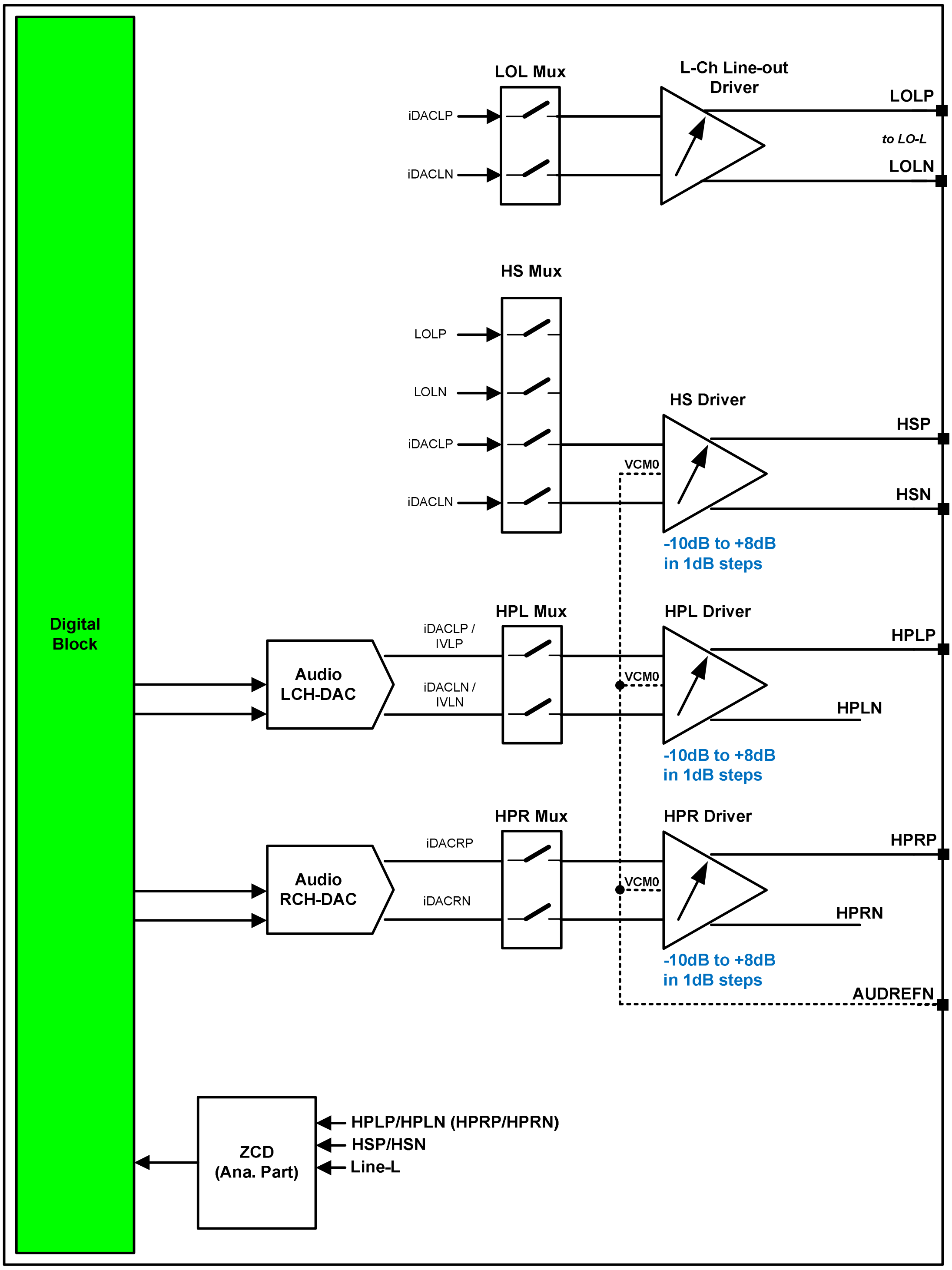

(b) Audio/speech downlink

Figure 3-3. Audio CODEC block diagram

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3.2.5.1.1 Charger Detection

A charger will be judged to be invalid when the charging source level is detected too high (> 10.5V) or too low (< 3.9V) to avoid improper charging behavior.

3.2.6 AUXADC

3.2.6.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the input channels. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 15-bit A/D converter: Converts the multiplexed input signal to 15-bit digital data..

Table 3-3. Application and input range of ADC channels

Channel	Application	Input range [V]
0	BATSNS	2.5 ~ 4.5
1	ISENSE	2.5 ~ 4.5
2	VCDT	0 ~ 1.5
3	BATON	0.05 ~ 2.8
5	ACCDET	0 ~ 1.8
6	N/A	0 ~ 1.8
7	AUXADC_VIN	0 ~ 3.3
others	Internal use	N/A

3.2.7 Fuel Gauge

The fuel gauging system includes a dedicated ADC for Li-Ion battery current measurement and utilizes the measurement ADC (AUXADC) for battery voltage and temperature measurement. The battery state-of-charge (SOC) estimation is performed by the software using the three measuring methods and the accumulated current measurement. The application diagram of the fuel gauging system is shown in the figure below, where an external resistor is used to convert the current drawn from the battery into a voltage which is then measured by FG ADC. The value of the external resistor must be chosen so that the maximum current during charging or discharging will not cause ADC to exceed its input voltage range.

The principle of operation of the fuel gauge relies on a combination of Coulomb counting and light load battery voltage measurement. Coulomb counting provides an estimate of the charge that has been withdrawn or delivered to the battery, while battery voltage measurement proves a good estimate of the battery SOC under low-load conditions. The battery voltage measurement compensates for error accumulation during the current integration inherent in Coulomb counting. The hardware also includes necessary modes to allow for simultaneous current and voltage measurement which can be utilized to estimate the battery impedance.

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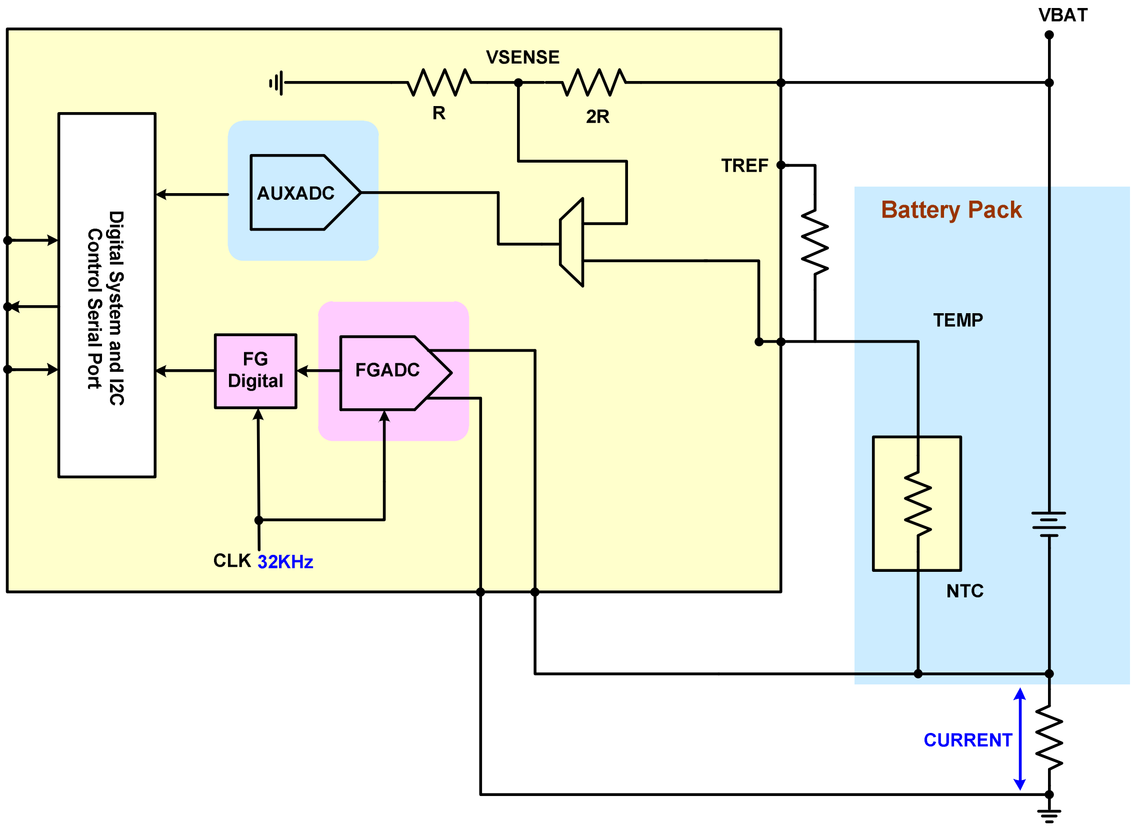

Figure 3-4. Fuel gauge block diagram and external connection

3.2.8 BIF

MIPI Battery Interface (BIF) is the first comprehensive battery communication interface standard for mobile devices. BIF module serves as a BIF master, which follows MIPI BIF protocol. It can be used to communicate with the battery package which has the BIF slave devices to monitor the battery status. Each transaction is started from a master and the slaves are the passive side.

Features:

- One wire communication
- Supports smart battery
- Single master, multi slave
- Receives at most 10 data packets in one transaction
- Sends at most 15 data packets in one transaction

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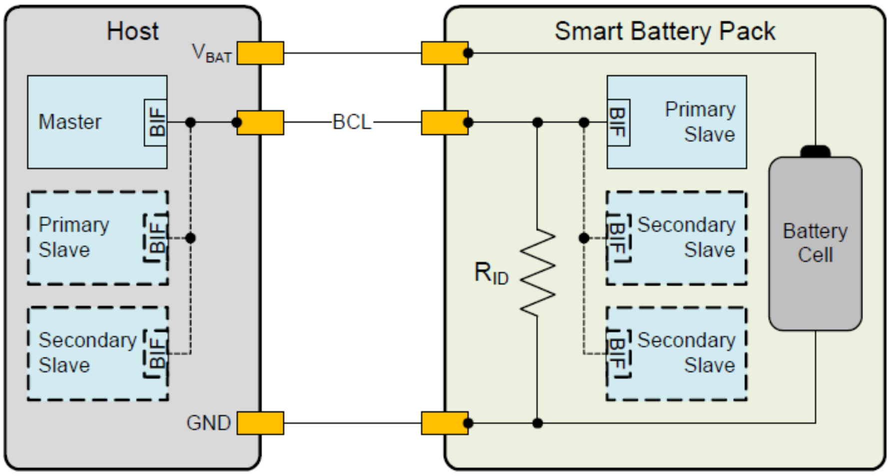

Figure 3-5. BIF application diagram

3.2.9 Real-time Clock

The Real Time Clock (RTC) module provides time and data information. The clock is based on a 32.768kHz oscillator with an independent power supply. When the mobile handset is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor will be used. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches a maximum value (e.g. 59 for seconds and minutes, 23 for hours, etc.). The year span is supported up to 2,127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

In MT6356, RTC module support function without 32kHz crystal. RTC module has an embedded 32kHz oscillator to assist life time extension after master 32kHz clock is off.

3.2.10 DCXO

3.2.10.1 Reference Clock Specification

MT6356 PMIC integrates a core 26MHz XTAL oscillator (XO) and supports 32kHz RTC-removal low power mode. It also provides backward compatible (BCM) configurations for previous solutions. There are two High Performance (1.8V_{PP}) and three Low Power (1.0V_{PP}) external clock buffers for the entire system and one internal buffer for audio.

The modes of operation are configured by two input pins, DCXO32K_EN and XMODE, and the definitions are shown as below.

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DCXO32K_EN	XMODE	Mode
LOW	LOW	Buffer mode with external TCXO
LOW	HIGH	NA
HIGH	LOW	BC M mode, system clock from RF
HIGH	HIGH	Oscillator mode without 32K RTC

In oscillator mode, the Temperature Sensing Crystal (TSX) is connected between XTAL1 and XTAL2. In buffer mode, the external clock inputs from XTAL1. Keep XTAL2 pin NC.
Note that DCXO32K_EN and XMODE are default high and can be programmed after the first power-on; after that MT6356 can select proper power-on-sequence for different system configurations.

3.2.10.2 Reference Output Buffer(s) Specification

There are five 26MHz clock output buffers driving out from the chip. They can be used as reference clocks for other chips and applications. Two High Performance (HP) external buffers output 0~1.8V squarer wave, and three Low Power (LP) external buffers output 0~1.0V squarer wave. Note that all their DC common mode voltage is not 0, so DC block capacitor is required if it is AC coupled and specific common mode voltage.

The current of all buffers can be optimized for different PCB Cloadings. Typical current consumption is optimized for < 20pF Cloading.

Parameter	Conditions	Min.	Nom.	Max.	Unit
Zload (Rp||Cp)	Rp	3			kΩ
	Cp			30	pF
Duty cycle		40		60	%
Rise/Fall time	10% to 90% of signal swing @ Cload=20pF			5	ns
HP buffer output	Square wave	1.6	1.8	2.0	Vp-p
HP SSB phase noise	1Hz offset [20pF load]			-50	dBc/Hz
	5Hz offset [20pF load]			-73	dBc/Hz
	10Hz offset [20pF load]			-80	dBc/Hz
	100Hz offset [20pF load]			-106	dBc/Hz
	1kHz offset [20pF load]			-134	dBc/Hz
	10kHz offset [20pF load]			-144	dBc/Hz
	100kHz offset [20pF load]			-152	dBc/Hz
HP current consumption	Zload = 20pF (each buffer)		2.0		mA
LP buffer output	Square wave	0.8	1.1	1.3	Vp-p
LP SSB phase noise	100Hz offset [20pF load]			-85	dBc/Hz
	1kHz offset [20pF load]			-110	dBc/Hz

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Parameter	Conditions	Min.	Nom.	Max.	Unit
	10kHz offset [20pF load]			-130	dBc/Hz
	100kHz offset [20pF load]			-130	dBc/Hz
LP current consumption	Zload = 20pF (each buffer)		1		mA

3.2.10.3 32kHz RTC Removal Mode

32kHz clock is produced by a fractional-N divider (1st order Sigma Delta Modulated).

Parameter	Conditions	Min.	Nom.	Max.	Unit
Frequency	Averaged value		32768		Hz
XO LPM current consumption	Low power mode With all capacitors switched off and auto-amplitude calibration on		75		µA
Duty cycle				70	%
Settling time				5	ms
Frequency variation	After system calibration			±2	ppm
	Over temperature -30°C to 85°C			15	ppm
	Uncalibrated – total variation			200	ppm

3.2.11 Interrupt and Watchdog

3.2.11.1 Interrupt

Here are interrupt lists of PMIC to inform BB IC:

1. Key pressed and released interrupt
   - PWRKEY: Interrupt is issued when PWRKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the PWRKEY_DEB status to see if it is pressed or released.
   - FCHR_ENB: Interrupt is issued when FCHR_ENB is pressed (and released, set by the register). After receiving the interrupt, the software will read the HOMEKEY _DEB status to see if it is pressed or released.
2. Thermal interrupt

   PMIC issues THR_H interrupt for the software high power latch if PMIC die temperature is over thermal regulation high threshold (e.g. 125°c) and issues THR_L for software latch release if PMIC die temperature goes from thermal regulation high threshold (e.g. 125°c) back to under thermal regulation low threshold (e.g. 110°c). The thermal regulation high/low threshold is adjustable.
3. Charger related interrupt
4. Battery voltage/current H/L interrupt

   There are two groups of VBAT detection interrupts.

   1) VBAT detected by AUXADC

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If VBAT is higher than the threshold specified by a register setting, the HIGHBATTERY interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the LOWBATTERY interrupt will be issued.

2) VBAT detected by fuel gauge
If VBAT is higher than the threshold specified by a register setting, the VBAT_H interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the VBAT_L interrupt will be issued.

5. Fuel-gauge
6. Buck OC interrupt
   There are six bucks and each has its individual interrupt which uses PWM detection method.
7. Buck PREOC interrupt
   There are one buck preoc interrupts for VCORE.
8. LDO OC interrupt
   PMIC supports LDO OC interrupt generation. It will be issued if any one of the LDOs has OC condition.
9. RTC interrupt
10. AUDIO interrupt
    Audio interrupt can inform AP playback of the audio status.
11. ACCDET interrupt
    This is for headphone detection.
12. Novel Adaptive Fuel Gauge (NAFG) delta-V accumulation interrupt
    If the accumulation of NAFG delta-voltage is larger than the programmable threshold, this interrupt will be issued.

3.2.11.2 Watchdog Reset

WDTRSTB_IN is the watchdog reset from AP. PMIC resets all modules to initial state when receiving watchdog reset from AP.

3.2.11.3 Booting Watchdog Reset

PMIC implements a booting watchdog function to prevent AP not booting up correctly. After all default on powers are turned on and RESETB is released, WDTRSTB_IN or PWRHOLD should be set high in a pre-determined time period or PMIC will shut down all powers and re-power on again if the PWRKEY or CHRIN power-on condition still exists.

3.2.12 SPI Interface

PMIC uses a 4-wire interface consisting of a clock, a chip select and two data signals (MOSI and MISO) to connect to BB. This serial-parallel interface allows BB to write commands to and read status from PMIC.

On the other hand, the IO pin (MISO) can be used as data pin or interrupt pin depending on what the system scenario is. It is used as data pin when system is in normal mode but as INT pin when system is in suspend mode.

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3.2.12.1 Data Format

The pre-defined SPI format consists of two modes: Single I/O mode and dual I/O mode. Single I/O always uses MOSI as output and input. Dual I/O uses both MOSI and MISO to be output and input to achieve better channel usage. The format conveys information of R/W direction, 15-bit address (bit15 to bit1) and 16-bit data, and both addresses and data are MSB first. The operation waveform of SPI is illustrated as below. The SPI slave in PMIC latch data sent from the master is at the rising edge of the clock, and output data are at the falling edge of the clock. The parameter tSLCH, tDMMY and tCHSH are fully configurable through command registers (in BB instead of PMIC) as illustrated in the figures below.

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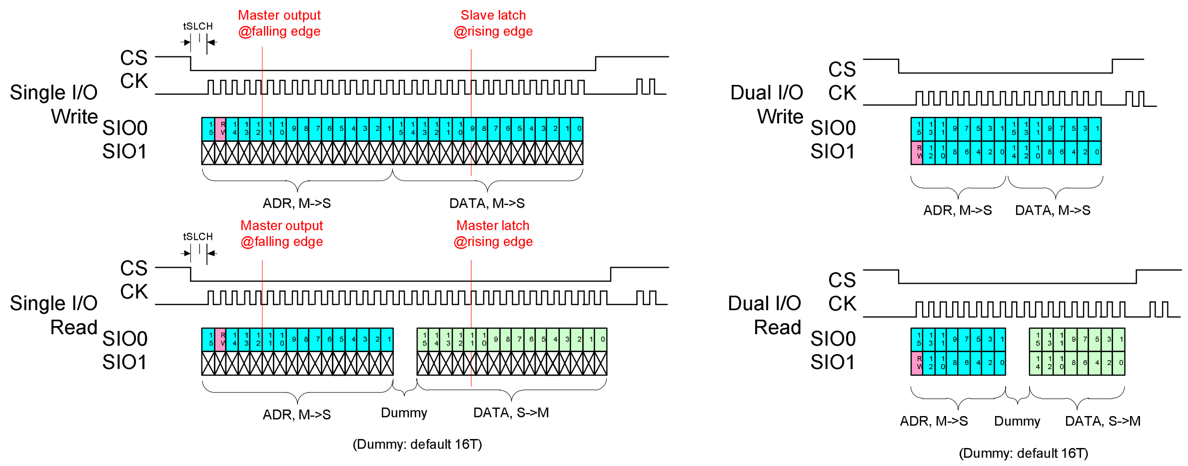
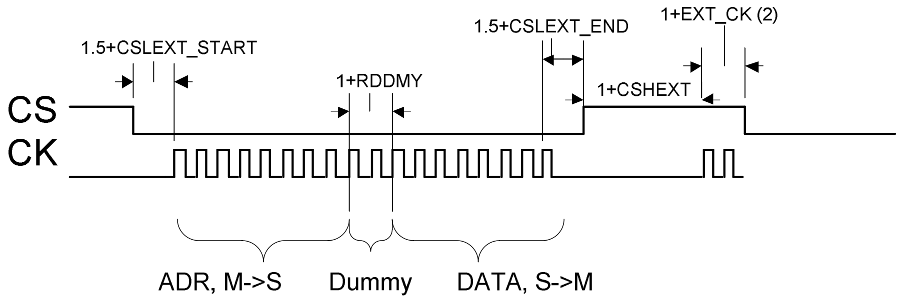
SPI format:



SPI parameter configuration:



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3.2.13 GPIO

3.2.13.1 GPIO List

Table 3-7. MT6356 GPIO list

Pin Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6	Aux Func.7	PU/PD
PAD_HOMEKEY	GPIO0	**I1:HOMEKEY**	O:INT_0			I0:TEST_CK0			**PU**/PD
PAD_SRCLKEN_IN0	GPIO1	**I1:SRCLKEN_IN0**					I0:TEST_IN0	O:TEST_OUT0	**PU**/PD
PAD_SRCLKEN_IN1	GPIO2	**I1:SRCLKEN_IN1**				I0:TEST_CK1	I0:TEST_IN1	O:TEST_OUT1	**PU**/PD
PAD_RTC32K_1V8_0	GPIO3	**O:RTC_32K1V8_0**				I0:TEST_CK2	I0:TEST_IN2	O:TEST_OUT2	PU/PD
PAD_RTC32K_1V8_1	GPIO4	**O:RTC_32K1V8_1**	O:INT_1	I0: EINT0			I0:TEST_IN3	O:TEST_OUT3	PU/PD
PAD_SCP_VREQ_VAO	GPIO5	**I0:SCP_VREQ_VAO**					I0:TEST_IN4	O:TEST_OUT4	PU/**PD**
PAD_SPI_CLK	GPIO6	**I0:SPI_CLK**							PU/**PD**
PAD_SPI_CSN	GPIO7	**I1:SPI_CSN**							**PU**/PD
PAD_SPI_MOSI	GPIO8	**B0:SPI_MOSI**							PU/PD
PAD_SPI_MISO	GPIO9	**B0:SPI_MISO**							PU/PD
PAD_AUD_CLK	GPIO10	**I0:AUD_CLK**		I0: EINT1			I0:TEST_IN5	O:TEST_OUT5	PU/**PD**
PAD_AUD_DAT_MOSI	GPIO11	**I0:AUD_DAT_MOSI**		I0: EINT2			I0:TEST_IN6	O:TEST_OUT6	PU/**PD**
PAD_AUD_DAT_MISO	GPIO12	**O:AUD_DAT_MISO**		I0: EINT3	O:VOW_DAT_MISO		I0:TEST_IN7	O:TEST_OUT7	PU/PD
PAD_VOW_CLK_MISO	GPIO13	**O:VOW_CLK_MISO**		I0: EINT4					PU/PD

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3.2.13.2 GPIO Specification

Table 3-8. MT6356 GPIO electrical characteristics

Paramters	Descriptions	Min.	Typ.	Max.	Unit
Inputs					
VIH	Input logic low voltage	0.75*VDDQ		VDDQ+0.3	V
VIL	Input logic high voltage	-0.3		0.25*VDDQ	V
Rpu	Input pull-up resistance	40	75	190	KΩ
Rpd	Input pull-down resistance	40	75	190	KΩ
Outputs					
VOH (DC)	DC Output logic low voltage	0.75*VDDQ			V
VOL (DC)	DC Output logic high voltage			0.25*VDDQ	V
Leakage					
IIN	Input leakage current (any input 0V < VIN < VDDIO)	-5		5	mA
IOZ	Tri-state output leakage current	-5		5	mA
IIN	Input leakage current (VIN=3.3V/0V) for floating nwell IO	-10		10	mA
IOZ	Tri-state output leakage current for for floating nwell IO	-10		10	mA

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3.3 Register Table and Descriptions

Module name: MT6356_PMIC_Register_Mapping_(E2) Base address: (+0h)

Address	Name	Width	Register Function
000A	PONSTS	16	Power On Source Record Register
000C	POFFSTS	16	Power Off Source Record Register
000E	PSTSCTL	16	Power On/Off Status Control
0014	PG_SDN_STS0	16	Power Good Shutdown Status 0
0016	PG_SDN_STS1	16	Power Good Shutdown Status 1
0018	OC_SDN_STS0	16	OC Shutdown Status 0
0156	TOP_RST_MISC	16	Reset Control Misc
019C	TOP_INT_STATUS0	16	TOP_INT_STATUS Register 0
020C	TOP_CLK_TRIM	16	TOP_CLK_TRIM Register
0294	RG_SPI_CON3	16	SPI Control Register 3
0296	RG_SPI_CON4	16	SPI Control Register 4
0298	RG_SPI_CON5	16	SPI Control Register 5
029A	RG_SPI_CON6	16	SPI Control Register 6
029C	RG_SPI_CON7	16	SPI Control Register 7
029E	RG_SPI_CON8	16	SPI Control Register 8
02D8	PSC_TOP_INT_STATUS0	16	PSC_TOP INT Status Register 0
0308	STRUP_ANA_CON1	16	STRUP Control Register 1
0346	PPCCTL0	16	PPC Control 0 Register
034C	PPCCFG0	16	PPC Configuration 0 Register
0374	STRUP_CON4	16	STRUP DIG Control Register N4
0376	STRUP_CON5	16	STRUP DIG Control Register N5
0384	STRUP_CON12	16	STRUP DIG Control Register 12
0386	STRUP_CON13	16	STRUP DIG Control Register 13
03C8	CHR_TOP_CON0	16	Charger Top Control Register 0
03CC	CHR_TOP_CON3	16	Charger Top Control Register 3
03CE	CHR_TOP_CON4	16	Charger Top Control Register 4
03D4	CHR_TOP_CON7	16	Charger Top Control Register 7
0408	CHR_CON0	16	Charger Control Register 0
040C	CHR_CON2	16	Charger Control Register 2
0418	CHR_CON8	16	Charger Control Register 8
042C	CHR_CON18	16	Charger Control Register 18
0446	BM_TOP_PAM0	16	BM_TOP Parameter 0
0448	BM_TOP_PAM1	16	BM_TOP Parameter 1
044A	BM_TOP_CLK_CON0	16	BM_TOP Clock Register 0
044C	BM_TOP_CKPDN_CON0	16	BM_TOP_CKPDN Control Register 0
044E	BM_TOP_CKPDN_CON0_SET	16	BM_TOP_CKPDN_CON0 Register SET
0450	BM_TOP_CKPDN_CON0_CLR	16	BM_TOP_CKPDN_CON0 Register CLR

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Address	Name	Width	Register Function
0452	**BM_TOP_CKSEL_CON0**	16	BM_TOP_CKSEL Control Register 0
0454	**BM_TOP_CKSEL_CON0_SET**	16	BM_TOP_CKSEL_CON0 Register SET
0456	**BM_TOP_CKSEL_CON0_CLR**	16	BM_TOP_CKSEL_CON0 Register CLR
0458	**BM_TOP_CKDIVSEL_CON0**	16	BM_TOP_CKDIVSEL Control Register 0
045A	**BM_TOP_CKDIVSEL_CON0_SET**	16	BM_TOP_CKDIVSEL_CON0 Register SET
045C	**BM_TOP_CKDIVSEL_CON0_CLR**	16	BM_TOP_CKDIVSEL_CON0 Register CLR
045E	**BM_TOP_CKHWEN_CON0**	16	BM_TOP_CKHWEN Control Register 0
0460	**BM_TOP_CKHWEN_CON0_SET**	16	BM_TOP_CKHWEN_CON0 Register SET
0462	**BM_TOP_CKHWEN_CON0_CLR**	16	BM_TOP_CKHWEN_CON0 Register CLR
0514	**FGADC_CUR_CON0**	16	FGADC_CUR Control Register 0
051C	**FGADC_CAR_CON0**	16	FGADC_CAR Control Register 0
051E	**FGADC_CAR_CON1**	16	FGADC_CAR Control Register 1
0530	**FGADC_NCAR_CON0**	16	FGADC_NCAR Control Register 0
0532	**FGADC_NCAR_CON1**	16	FGADC_NCAR Control Register 1
0538	**FGADC_IAVG_CON0**	16	FGADC_IAVG Control Register 0
053A	**FGADC_IAVG_CON1**	16	FGADC_IAVG Control Register 1
0544	**FGADC_NTER_CON0**	16	FGADC_NTER Control Register 0
0546	**FGADC_NTER_CON1**	16	FGADC_NTER Control Register 1
0606	**BATON_ANA_CON0**	16	BATON Analog Control Register 0
0686	**BIF_CON0**	16	BIF Control Register 0
0688	**BIF_CON1**	16	BIF Control Register 1
068A	**BIF_CON2**	16	BIF Control Register 2
068C	**BIF_CON3**	16	BIF Control Register 3
068E	**BIF_CON4**	16	BIF Control Register 4
0690	**BIF_CON5**	16	BIF Control Register 5
0692	**BIF_CON6**	16	BIF Control Register 6
0694	**BIF_CON7**	16	BIF Control Register 7
0696	**BIF_CON8**	16	BIF Control Register 8
0698	**BIF_CON9**	16	BIF Control Register 9
069A	**BIF_CON10**	16	BIF Control Register 10
069C	**BIF_CON11**	16	BIF Control Register 11
069E	**BIF_CON12**	16	BIF Control Register 12
06A0	**BIF_CON13**	16	BIF Control Register 13

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Address	Name	Width	Register Function
06A2	**BIF_CON14**	16	BIF Control Register 14
06A4	**BIF_CON15**	16	BIF Control Register 15
06A6	**BIF_CON16**	16	BIF Control Register 16
06A8	**BIF_CON17**	16	BIF Control Register 17
06AA	**BIF_CON18**	16	BIF Control Register 18
06AC	**BIF_CON19**	16	BIF Control Register 19
06AE	**BIF_CON20**	16	BIF Control Register 20
06B0	**BIF_CON21**	16	BIF Control Register 21
06B2	**BIF_CON22**	16	BIF Control Register 22
06B4	**BIF_CON23**	16	BIF Control Register 23
06B6	**BIF_CON24**	16	BIF Control Register 24
06B8	**BIF_CON25**	16	BIF Control Register 25
06BA	**BIF_CON26**	16	BIF Control Register 26
06BC	**BIF_CON27**	16	BIF Control Register 27
06BE	**BIF_CON28**	16	BIF Control Register 28
06C0	**BIF_CON29**	16	BIF Control Register 29
06C4	**BIF_CON31**	16	BIF Control Register 31
06C6	**BIF_CON32**	16	BIF Control Register 32
06D0	**BIF_CON37**	16	BIF Control Register 37
06D2	**BIF_CON38**	16	BIF Control Register 38
0786	**AUXADC_ADC0**	16	AUXADC ADC Register 0
0788	**AUXADC_ADC1**	16	AUXADC ADC Register 1
078A	**AUXADC_ADC2**	16	AUXADC ADC Register 2
078C	**AUXADC_ADC3**	16	AUXADC ADC Register 3
078E	**AUXADC_ADC4**	16	AUXADC ADC Register 4
0790	**AUXADC_ADC5**	16	AUXADC ADC Register 5
0792	**AUXADC_ADC6**	16	AUXADC ADC Register 6
0794	**AUXADC_ADC7**	16	AUXADC ADC Register 7
0796	**AUXADC_ADC8**	16	AUXADC ADC Register 8
0798	**AUXADC_ADC9**	16	AUXADC ADC Register 9
079A	**AUXADC_ADC10**	16	AUXADC ADC Register 10
079C	**AUXADC_ADC11**	16	AUXADC ADC Register 11
079E	**AUXADC_ADC12**	16	AUXADC ADC Register 12
07A0	**AUXADC_ADC13**	16	AUXADC ADC Register 13
07A2	**AUXADC_ADC14**	16	AUXADC ADC Register 14
07A4	**AUXADC_ADC15**	16	AUXADC ADC Register 15
07A6	**AUXADC_ADC16**	16	AUXADC ADC Register 16
07A8	**AUXADC_ADC17**	16	AUXADC ADC Register 17
07AA	**AUXADC_ADC18**	16	AUXADC ADC Register 18
07AC	**AUXADC_ADC19**	16	AUXADC ADC Register 19
07AE	**AUXADC_ADC20**	16	AUXADC ADC Register 20
07B0	**AUXADC_ADC21**	16	AUXADC ADC Register 21
07B2	**AUXADC_ADC22**	16	AUXADC ADC Register 22
07B4	**AUXADC_ADC23**	16	AUXADC ADC Register 23
07B6	**AUXADC_ADC24**	16	AUXADC ADC Register 24

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Address	Name	Width	Register Function
07B8	AUXADC_ADC25	16	AUXADC ADC Register 25
07BA	AUXADC_ADC26	16	AUXADC ADC Register 26
07BC	AUXADC_ADC27	16	AUXADC ADC Register 27
07BE	AUXADC_ADC28	16	AUXADC ADC Register 28
07C0	AUXADC_ADC29	16	AUXADC ADC Register 29
07C2	AUXADC_ADC30	16	AUXADC ADC Register 30
07C4	AUXADC_ADC31	16	AUXADC ADC Register 31
07C6	AUXADC_ADC32	16	AUXADC ADC Register 32
07C8	AUXADC_ADC33	16	AUXADC ADC Register 33
07CA	AUXADC_ADC34	16	AUXADC ADC Register 34
07CC	AUXADC_ADC35	16	AUXADC ADC Register 35
07CE	AUXADC_ADC36	16	AUXADC ADC Register 36
07D0	AUXADC_ADC37	16	AUXADC ADC Register 37
07DA	AUXADC_ADC42	16	AUXADC ADC Register 42
07DC	AUXADC_ADC43	16	AUXADC ADC Register 43
07DE	AUXADC_ADC44	16	AUXADC ADC Register 44
07E0	AUXADC_ADC45	16	AUXADC ADC Register 45
07E2	AUXADC_ADC46	16	AUXADC ADC Register 46
07E4	AUXADC_ADC47	16	AUXADC ADC Register 47
07E6	AUXADC_STA0	16	AUXADC_STA0
07E8	AUXADC_STA1	16	AUXADC_STA1
07EA	AUXADC_STA2	16	AUXADC_STA2
0992	SCK_TOP_CKPDN_CON0	16	SCK_CKPDN Control Register 0
0994	SCK_TOP_CKPDN_CON0_SET	16	SCK_CKPDN Control Register 0 SET
0996	SCK_TOP_CKPDN_CON0_CLR	16	SCK_CKPDN Control Register 0 CLR
0998	SCK_TOP_CKHWEN_CON0	16	SCK_CKHWEN Control Register 0
099A	SCK_TOP_CKHWEN_CON0_SET	16	SCK_CKHWEN_CON Register 0 SET
099C	SCK_TOP_CKHWEN_CON0_CLR	16	SCK_CKHWEN_CON Register 0 CLR
09C6	DCXO_CW00	16	DCXO Code Word 0
09C8	DCXO_CW00_SET	16	DCXO Code Word 0 Set
09CA	DCXO_CW00_CLR	16	DCXO Code Word 0 Clear
09CC	DCXO_CW01	16	DCXO Code Word 1
09CE	DCXO_CW02	16	DCXO Code Word 2
09D0	DCXO_CW03	16	DCXO Code Word 3
09D2	DCXO_CW04	16	DCXO Code Word 4
09D4	DCXO_CW05	16	DCXO Code Word 5
09D6	DCXO_CW06	16	DCXO Code Word 6
09D8	DCXO_CW07	16	DCXO Code Word 7
09DA	DCXO_CW08	16	DCXO Code Word 8
09DC	DCXO_CW09	16	DCXO Code Word 9

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Address	Name	Width	Register Function
09DE	DCXO_CW10	16	DCXO Code Word 10
09E0	DCXO_CW11	16	DCXO Code Word 11
09E2	DCXO_CW11_SET	16	DCXO Code Word 11 Set
09E4	DCXO_CW11_CLR	16	DCXO Code Word 11 Clear
09E6	DCXO_CW12	16	DCXO Code Word 12
09E8	DCXO_CW13	16	DCXO Code Word 13
09EA	DCXO_CW14	16	DCXO Code Word 14
09EC	DCXO_CW15	16	DCXO Code Word 15
09EE	DCXO_CW16	16	DCXO Code Word 16
09F0	DCXO_CW17	16	DCXO Code Word 17
09F2	DCXO_CW18	16	DCXO Code Word 18
09F4	DCXO_CW19	16	DCXO Code Word 19
09F6	DCXO_CW20	16	DCXO Code Word 20
09F8	DCXO_CW21	16	DCXO Code Word 21
09FA	DCXO_CW22	16	DCXO Code Word 22
09FE	DCXO_ELR0	16	DCXO ELR 0 Register
0A08	RTC_BBPU	16	Baseband Power Up
0A0A	RTC_IRQ_STA	16	**RTC IRQ Status** This register is fixed in 0 when RTC_POWERKEY1 & RTC_POWERKEY2 unmatch the correct values.
0A0C	RTC_IRQ_EN	16	**RTC IRQ Enable** This register is fixed in 0 when RTC_POWERKEY1 & RTC_POWERKEY2 unmatch the correct values.
0A0E	RTC_CII_EN	16	**Counter Increment IRQ Enable** This register activates or de-activates the IRQ generation when the TC counter reaches its maximum value.
0A10	RTC_AL_MASK	16	**RTC Alarm Mask** The alarm condition for alarm IRQ generation depends on whether or not the corresponding bit in this register is masked. Warning: If you set all bits 1 in RTC_AL_MASK (i.e. RTC_AL_MASK=0x7f) and PWREN=1 in RTC_BBPU, it means alarm comes EVERY SECOND, not disabled.
0A12	RTC_TC_SEC	16	RTC Seconds Time Counter Register
0A14	RTC_TC_MIN	16	RTC Minutes Time Counter Register
0A16	RTC_TC_HOU	16	RTC Hours Time Counter Register
0A18	RTC_TC_DOM	16	RTC Day-of-month Time Counter Register
0A1A	RTC_TC_DOW	16	RTC Day-of-Week time Counter Register
0A1C	RTC_TC_MTH	16	RTC Month Time Counter Register
0A1E	RTC_TC_YEA	16	RTC Year Time Counter Register
0A20	RTC_AL_SEC	16	RTC Second Alarm Setting Register
0A22	RTC_AL_MIN	16	RTC Minute Alarm Setting Register
0A24	RTC_AL_HOU	16	RTC Hour Alarm Setting Register
0A26	RTC_AL_DOM	16	RTC Day-of-month Alarm Setting Register
0A28	RTC_AL_DOW	16	RTC Day-of-week Alarm Setting Register
0A2A	RTC_AL_MTH	16	RTC Month Alarm Setting Register
0A2C	RTC_AL_YEA	16	RTC Year Alarm Setting Register
0A2E	RTC_OSC32CON	16	**OSC32 Control** The function is only active when RTC_POWERKEY1 & RTC_POWERKEY2 match the correct values. When

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Address	Name	Width	Register Function
			powerkeys do not match, the internal xosccali=0x7.
0A30	RTC_POWERKEY1	16	RTC_POWERKEY1 Register
0A32	RTC_POWERKEY2	16	RTC_POWERKEY2 Register
0A34	RTC_PDN1	16	PDN1
0A36	RTC_PDN2	16	PDN2
0A38	RTC_SPAR0	16	Spare Register for Specific Purpose 0
0A3A	RTC_SPAR1	16	Spare Register for Specific Purpose 1
0A3C	RTC_PROT	16	Lock/Unlock Scheme to Prevent RTC Miswriting
0A3E	RTC_DIFF	16	**One-time Calibration Offset** This register is fixed in 0 when RTC_POWERKEY1 & RTC_POWERKEY2 unmatch the correct values.
0A40	RTC_CALI	16	**Repeat Calibration Offset** This register is fixed in 0 when RTC_POWERKEY1 & RTC_POWERKEY2 unmatch the correct values.
0A42	RTC_WRTGR	16	Enable Transfers from Core to RTC in Queue
0A44	RTC_CON	16	**Other RTC Control Register** Note: GPU,GOE,LPRST,LPEN and GPEN are tie0 and F32KOB is tie1 internally when RTC_POWERKEY1 & RTC_POWERKEY2 do not match the correct values. After changing the RTC_CON, you have to write WRTGR=1 to take effect.
0AC8	RTC_TC_SEC_SEC	16	Security RTC Seconds Time Counter Register
0ACA	RTC_TC_MIN_SEC	16	Security RTC Minutes Time Counter Register
0ACC	RTC_TC_HOU_SEC	16	Security RTC Hours Time Counter Register
0ACE	RTC_TC_DOM_SEC	16	Security RTC Day-of-month Time Counter Register
0AD0	RTC_TC_DOW_SEC	16	Security RTC Day-of-week Time Counter Register
0AD2	RTC_TC_MTH_SEC	16	Security RTC Month Time Counter Register
0AD4	RTC_TC_YEA_SEC	16	Security RTC Year Time Counter Register
0AD6	RTC_SEC_CK_PDN	16	Security RTC Clock Control Register
0AD8	RTC_SEC_WRTGR	16	Enable Transfers from Core to Security RTC in Queue
0B3A	BUCK_TOP_OC_CON0	16	BUCK_TOP OC Control Register 0
0B86	BUCK_VPROC_CON0	16	BUCK VPROC Control 0
0BA8	BUCK_VPROC_ELR0	16	BUCK_VPROC ELR 0 Register
0BC6	BUCK_VCORE_CON0	16	BUCK VCORE Control 0
0BE8	BUCK_VCORE_ELR0	16	BUCK_VCORE ELR 0 Register
0C06	BUCK_VMODEM_CON0	16	BUCK VMODEM Control 0
0C30	BUCK_VMODEM	16	BUCK_VMODEM ELR 0 Register

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Address	Name	Width	Register Function
	_ELR0		
0C46	BUCK_VS1_CON0	16	BUCK VS1 Control 0
0C6C	BUCK_VS1_VOTER_CFG	16	BUCK VS1 VOTER Configure
0C86	BUCK_VS2_CON0	16	BUCK VS2 Control 0
0CAC	BUCK_VS2_VOTER_CFG	16	BUCK VS2 VOTER Configure
0CC6	BUCK_VPA_CON0	16	BUCK VPA Control 0
0CC8	BUCK_VPA_CON1	16	BUCK VPA Control 1
0D18	VCORE_VPROC_ANA_CON5	16	VCORE_VPROC Control Register 5
0D24	VCORE_VPROC_ANA_CON11	16	VCORE_VPROC Control Register 11
0D34	VMODEM_ANA_CON7	16	VMODEM Control Register 7
0D3E	VS1_ANA_CON4	16	VS1 Control Register 4
0D4A	VS2_ANA_CON4	16	VS2 Control Register 4
0D58	VPA_ANA_CON5	16	VPA Control Register 5
0D6A	SMPS_ELR_7	16	SMPS ELR 7 Register
0D8A	LDO_TOP_CLK_DCM_CON0	16	LDO DCM Control Register 0
0D8C	LDO_TOP_CLK_VIO28_CON0	16	LDO VIO28 Clock Gating Control Register 0
0D8E	LDO_TOP_CLK_VIO18_CON0	16	LDO VIO18 Clock Gating Control Register 0
0D90	LDO_TOP_CLK_VAUD28_CON0	16	LDO VAUD28 Clock Gating Control Register 0
0D92	LDO_TOP_CLK_VDRAM_CON0	16	LDO VDRAM Clock Gating Control Register 0
0D94	LDO_TOP_CLK_VA12_CON0	16	LDO VA12 Clock Gating Control Register 0
0D96	LDO_TOP_CLK_VSRAM_PROC_CON0	16	LDO VSRAM_PROC Clock Gating Control Register 0
0D98	LDO_TOP_CLK_VSRAM_OTHERS_CON0	16	LDO VSRAM_OTHERS Clock Gating Control Register 0
0D9A	LDO_TOP_CLK_VSRAM_GPU_CON0	16	LDO VSRAM_GPU Clock Gating Control Register 0
0D9C	LDO_TOP_CLK_VAUX18_CON0	16	LDO VAUX18 Clock Gating Control Register 0
0D9E	LDO_TOP_CLK_VUSB_CON0	16	LDO VUSB Clock Gating Control Register 0
0DA0	LDO_TOP_CLK_VEMC_CON0	16	LDO VEMC Clock Gating Control Register 0
0DA2	LDO_TOP_CLK_VXO22_CON0	16	LDO VXO22 Clock Gating Control Register 0
0DA4	LDO_TOP_CLK_VSIM1_CON0	16	LDO VSIM1 Clock Gating Control Register 0
0DA6	LDO_TOP_CLK_	16	LDO VSIM2 Clock Gating Control Register 0

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Address	Name	Width	Register Function
	VSIM2_CON0		
0DA8	LDO_TOP_CLK_VCAMD_CON0	16	LDO VCAMD Clock Gating Control Register 0
0DAA	LDO_TOP_CLK_VCAMIO_CON0	16	LDO VCAMIO Clock Gating Control Register 0
0DAC	LDO_TOP_CLK_VMIPI_CON0	16	LDO VMIPI Clock Gating Control Register 0
0DAE	LDO_TOP_CLK_VCN33_CON0	16	LDO VCN33 Clock Gating Control Register 0
0DB0	LDO_TOP_CLK_VCN18_CON0	16	LDO VCN18 Clock Gating Control Register 0
0DB2	LDO_TOP_CLK_VCN28_CON0	16	LDO VCN28 Clock Gating Control Register 0
0DB4	LDO_TOP_CLK_VIBR_CON0	16	LDO VIBR Clock Gating Control Register 0
0DB6	LDO_TOP_CLK_VBIF28_CON0	16	LDO VBIF28 Clock Gating Control Register 0
0DB8	LDO_TOP_CLK_VFE28_CON0	16	LDO VFE28 Clock Gating Control Register 0
0DBA	LDO_TOP_CLK_VMCH_CON0	16	LDO VMCH Clock Gating Control Register 0
0DBC	LDO_TOP_CLK_VMC_CON0	16	LDO VMC Clock Gating Control Register 0
0DBE	LDO_TOP_CLK_VRF18_CON0	16	LDO VRF18 Clock Gating Control Register 0
0DC0	LDO_TOP_CLK_VLDO28_CON0	16	LDO VLDO28 Clock Gating Control Register 0
0DC2	LDO_TOP_CLK_VRF12_CON0	16	LDO VRF12 Clock Gating Control Register 0
0DC4	LDO_TOP_CLK_VCAMA_CON0	16	LDO VCAMA Clock Gating Control Register 0
0E18	LDO_VXO22_CON1	16	LDO VXO22 Control Register 1
0E2C	LDO_VA12_CON1	16	LDO VA12 Control Register 1
0E40	LDO_VAUX18_CON1	16	LDO VAUX18 Control Register 1
0E54	LDO_VAUD28_CON1	16	LDO VAUD28 Control Register 1
0E68	LDO_VIO28_CON1	16	LDO VIO28 Control Register 1
0E7C	LDO_VIO18_CON1	16	LDO VIO18 Control Register 1
0E90	LDO_VDRAM_CON1	16	LDO VDRAM Control Register 1
0EA4	LDO_VEMC_CON1	16	LDO VEMC Control Register 1
0F0A	LDO_VFE28_CON0	16	LDO VFE28 Control Register 0
0F18	LDO_VFE28_CON1	16	LDO VFE28 Control Register 1
0F1E	LDO_VRF18_CON0	16	LDO VRF18 Control Register 0
0F2C	LDO_VRF18_CON1	16	LDO VRF18 Control Register 1

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Address	Name	Width	Register Function
0F32	LDO_VRF12_CON0	16	LDO VRF12 Control Register 0
0F40	LDO_VRF12_CON1	16	LDO VRF12 Control Register 1
0F46	LDO_VMIPI_CON0	16	LDO VMIPI Control Register 0
0F54	LDO_VMIPI_CON1	16	LDO VMIPI Control Register 1
0F5A	LDO_VCN18_CON0	16	LDO VCN18 Control Register 0
0F68	LDO_VCN18_CON1	16	LDO VCN18 Control Register 1
0F6E	LDO_VCAMA_CON0	16	LDO VCAMA Control Register 0
0F7C	LDO_VCAMA_CON1	16	LDO VCAMA Control Register 1
0F82	LDO_VCAMD_CON0	16	LDO VCAMD Control Register 0
0F90	LDO_VCAMD_CON1	16	LDO VCAMD Control Register 1
0F96	LDO_VCAMIO_CON0	16	LDO VCAMIO Control Register 0
0FA4	LDO_VCAMIO_CON1	16	LDO VCAMIO Control Register 1
0FAA	LDO_VMC_CON0	16	LDO VMC Control Register 0
0FB8	LDO_VMC_CON1	16	LDO VMC Control Register 1
0FBE	LDO_VMCH_CON0	16	LDO VMCH Control Register 0
0FCC	LDO_VMCH_CON1	16	LDO VMCH Control Register 1
0FD0	LDO_VMCH_CON3	16	LDO VMCH control register 3
0FD2	LDO_VSIM1_CON0	16	LDO VSIM1 Control Register 0
0FE0	LDO_VSIM1_CON1	16	LDO VSIM1 Control Register 1
0FE6	LDO_VSIM2_CON0	16	LDO VSIM2 Control Register 0
0FF4	LDO_VSIM2_CON1	16	LDO VSIM2 Control Register 1
100A	LDO_VIBR_CON0	16	LDO VIBR Control Register 0
1018	LDO_VIBR_CON1	16	LDO VIBR Control Register 1
101E	LDO_VBIF28_CON0	16	LDO VBIF28 Control Register 0
102C	LDO_VBIF28_CON1	16	LDO VBIF28 Control Register 1
104A	LDO_VCN33_CON0_0	16	LDO VCN33 BT Control Register 0
1058	LDO_VCN33_CON0_1	16	LDO VCN33 WiFi Control Register 0
105A	LDO_VCN33_CON1	16	LDO VCN33 Control Register 1
1060	LDO_VLDO28_C	16	LDO VLDO28 AF Control Register 0

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Address	Name	Width	Register Function
	ON0_0		
106E	LDO_VLDO28_CON0_1	16	LDO VLDO28 TP Control Register 0
1070	LDO_VLDO28_CON1	16	LDO VLDO28 Control Register 1
1076	LDO_VUSB_CON0_0	16	LDO VUSB 0 Control Register 0
1084	LDO_VUSB_CON0_1	16	LDO VUSB 1 Control Register 0
1086	LDO_VUSB_CON1	16	LDO VUSB Control Register 1
10CA	LDO_VCN28_CON0	16	LDO VCN28 Control Register 0
10D8	LDO_VCN28_CON1	16	LDO VCN28 Control Register 1
111E	LDO_VSRAM_PROC_CON3	16	LDO VSRAM_PROC Control Register 3
1126	LDO_VSRAM_PROC_DBG1	16	LDO VSRAM_PROC DEBUG 1
113C	LDO_VSRAM_OTHERS_CON3	16	LDO VSRAM_OTHERS Control Register 3
1144	LDO_VSRAM_OTHERS_DBG1	16	LDO VSRAM_OTHERS DEBUG 1
115A	LDO_VSRAM_GPU_CON3	16	LDO VSRAM_GPU Control Register 3
1162	LDO_VSRAM_GPU_DBG1	16	LDO VSRAM_GPU DEBUG 1
1188	LDO_VSRAM_CON0	16	LDO VSRAM CONTROL 0
120A	VRTC_CON0	16	VRTC Control Register 0
1246	VCAMA_ANA_CON0	16	VCAMA Control Register 0
124A	VFE28_ANA_CON0	16	VFE28 Control Register 0
124E	VCN28_ANA_CON0	16	VCN28 Control Register 0
1252	VBIF28_ANA_CON0	16	VBIF28 Control Register 0
1262	VCN33_ANA_CON0	16	VCN33 Control Register 0
126E	VLDO28_ANA_CON0	16	VLDO28 Control Register 0
1276	VIBR_ANA_CON0	16	VIBR Control Register 0
127A	VSIM1_ANA_CON0	16	VSIM1 Control Register 0
127E	VSIM2_ANA_CON0	16	VSIM2 Control Register 0
1282	VMCH_ANA_CON0	16	VMCH Control Register 0
1286	VMC_ANA_CON0	16	VMC Control Register 0
128A	VCAMIO_ANA_CON0	16	VCAMIO Control Register 0
128E	VCN18_ANA_CO	16	VCN18 Control Register 0

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Address	Name	Width	Register Function
	N0		
1292	VRF18_ANA_CON0	16	VRF18 Control Register 0
129A	VMIPI_ANA_CON0	16	VMIPI Control Register 0
12A2	VRF12_ANA_CON0	16	VRF12 Control Register 0
12B0	CAMD_ANA_CON0	16	CAMD Control Register 0
134E	XPP_TOP_CKPDN_CON0	16	XPP_TOP_CKPDN Control Register 0
1350	XPP_TOP_CKPDN_CON0_SET	16	XPP_TOP_CKPDN_CON0 Register SET
1352	XPP_TOP_CKPDN_CON0_CLR	16	XPP_TOP_CKPDN_CON0 Register CLR
1354	XPP_TOP_CKSEL_CON0	16	XPP_TOP_CKSEL Control Register 0
1356	XPP_TOP_CKSEL_CON0_SET	16	XPP_TOP_CKSEL_CON0 Register SET
1358	XPP_TOP_CKSEL_CON0_CLR	16	XPP_TOP_CKSEL_CON0 Register CLR
135A	XPP_TOP_CKDIVSEL_CON0	16	XPP_TOP_CKDIVSEL Control Register 0
135C	XPP_TOP_CKDIVSEL_CON0_SET	16	XPP_TOP_CKDIVSEL_CON0 Register SET
135E	XPP_TOP_CKDIVSEL_CON0_CLR	16	XPP_TOP_CKDIVSEL_CON0 Register CLR
1360	XPP_TOP_CKHWEN_CON0	16	XPP_TOP_CKHWEN Control Register 0
1362	XPP_TOP_CKHWEN_CON0_SET	16	XPP_TOP_CKHWEN_CON0 Register SET
1364	XPP_TOP_CKHWEN_CON0_CLR	16	XPP_TOP_CKHWEN_CON0 Register CLR
154A	AUD_TOP_CKPDN_CON0	16	AUDIO CLK Power Down Register 0
154C	AUD_TOP_CKSEL_CON0	16	AUDIO CKSEL Control Register 0
1566	AUDNCP_CLKDIV_CON0	16	AUDNCP_CLKDIV Control Register 0
1568	AUDNCP_CLKDIV_CON1	16	AUDNCP_CLKDIV Control Register 1
156A	AUDNCP_CLKDIV_CON2	16	AUDNCP_CLKDIV Control Register 2
156C	AUDNCP_CLKDIV_CON3	16	AUDNCP_CLKDIV Control Register 3
156E	AUDNCP_CLKDIV_CON4	16	AUDNCP_CLKDIV Control Register 4
1570	AUD_TOP_MON_CON0	16	AUD_TOP_MON control register 0
1586	AFE_UL_DL_CON0	16	Audio UL and DL Control Register 0
1588	AFE_DL_SRC2_CON0_L	16	AFE_DL_SRC2 Control Register 0 Low Part
158A	AFE_UL_SRC_CON0_H	16	AFE Uplink SRC Control Register 0 High Part

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Address	Name	Width	Register Function
158C	AFE_UL_SRC_CON0_L	16	AFE Uplink SRC Control Register 0 Low Part
158E	AFE_TOP_CON0	16	AFE Top Control Register 0
1590	AUDIO_TOP_CON0	16	AUDIO Top Control Register 0
1592	AFE_MON_DEBUG0	16	AFE Monitor Output Debug Register 0
1594	AFUNC_AUD_CON0	16	A_FUNC AUDIO Control Register 0
1596	AFUNC_AUD_CON1	16	A_FUNC AUDIO Control Register 1
1598	AFUNC_AUD_CON2	16	A_FUNC AUDIO Control Register 2
159A	AFUNC_AUD_CON3	16	A_FUNC AUDIO Control Register 3
159C	AFUNC_AUD_CON4	16	A_FUNC AUDIO Control Register 4
159E	AFUNC_AUD_MON0	16	A_FUNC AUDIO Monitor Register 0
15A0	AUDRC_TUNE_MON0	16	Analog Monitor Register 0
15BA	AFE_SGEN_CFG0	16	AFE SGEN CON0
15BC	AFE_SGEN_CFG1	16	**AFE SGEN CON1** Sets up SGEN tone freq.
15BE	AFE_ADC_ASYNC_FIFO_CFG	16	AFE_ADC_SYNC_FIFO_CFG
15C0	AFE_DCCLK_CFG0	16	AFE_DCCLK_CFG0
15C2	AFE_DCCLK_CFG1	16	AFE_DCCLK_CFG1
1606	AUDENC_ANA_CON0	16	AUDENC Control Register 0
1608	AUDENC_ANA_CON1	16	AUDENC Control Register 1
160A	AUDENC_ANA_CON2	16	AUDENC Control Register 2
160C	AUDENC_ANA_CON3	16	AUDENC Control Register 3
160E	AUDENC_ANA_CON4	16	AUDENC Control Register 4
1610	AUDENC_ANA_CON5	16	AUDENC Control Register 5
1612	AUDENC_ANA_CON6	16	AUDENC Control Register 6
1614	AUDENC_ANA_CON7	16	AUDENC Control Register 7
1616	AUDENC_ANA_CON8	16	AUDENC Control Register 8
1618	AUDENC_ANA_CON9	16	AUDENC Control Register 9
161A	AUDENC_ANA_CON10	16	AUDENC Control Register 10
161C	AUDENC_ANA_CON11	16	AUDENC Control Register 11

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Address	Name	Width	Register Function
161E	AUDENC_ANA_CON12	16	AUDENC Control Register 12
1646	AUDDEC_ANA_CON0	16	AUDDEC Control Register 0
1648	AUDDEC_ANA_CON1	16	AUDDEC Control Register 1
164A	AUDDEC_ANA_CON2	16	AUDDEC Control Register 2
164C	AUDDEC_ANA_CON3	16	AUDDEC Control Register 3
164E	AUDDEC_ANA_CON4	16	AUDDEC Control Register 4
1650	AUDDEC_ANA_CON5	16	AUDDEC Control Register 5
1652	AUDDEC_ANA_CON6	16	AUDDEC Control Register 6
1654	AUDDEC_ANA_CON7	16	AUDDEC Control Register 7
1656	AUDDEC_ANA_CON8	16	AUDDEC Control Register 8
1658	AUDDEC_ANA_CON9	16	AUDDEC Control Register 9
165A	AUDDEC_ANA_CON10	16	AUDDEC Control Register 10
165C	AUDDEC_ANA_CON11	16	AUDDEC Control Register 11
165E	AUDDEC_ANA_CON12	16	AUDDEC Control Register 12
1660	AUDDEC_ANA_CON13	16	AUDDEC Control Register 13
1662	AUDDEC_ANA_CON14	16	AUDDEC Control Register 14
1664	AUDDEC_ANA_CON15	16	AUDDEC Control Register 15
1668	AUDDEC_ELR_0	16	AUDDEC ELR 0 Register
1686	ZCD_CON0	16	ZCD Control Register 0
1688	ZCD_CON1	16	ZCD Control Register 1
168A	ZCD_CON2	16	ZCD Control Register 2
168C	ZCD_CON3	16	ZCD Control Register 3
168E	ZCD_CON4	16	ZCD Control Register 4
1690	ZCD_CON5	16	ZCD Control Register 5
16C6	ACCDET_CON0	16	ACCDET Control Register 0
16C8	ACCDET_CON1	16	ACCDET Control Register 1
16CA	ACCDET_CON2	16	ACCDET Control Register 2
16CC	ACCDET_CON3	16	ACCDET Control Register 3
16CE	ACCDET_CON4	16	ACCDET Control Register 4
16D0	ACCDET_CON5	16	ACCDET Control Register 5
16D2	ACCDET_CON6	16	ACCDET Control Register 6
16D4	ACCDET_CON7	16	ACCDET Control Register 7
16D6	ACCDET_CON8	16	ACCDET Control Register 8
16D8	ACCDET_CON9	16	ACCDET Control Register 9

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Address	Name	Width	Register Function
16DA	ACCDET_CON10	16	ACCDET Control Register 10
16DE	ACCDET_CON12	16	ACCDET Control Register 12
16E2	ACCDET_CON14	16	ACCDET Control Register 14
16E4	ACCDET_CON15	16	ACCDET Control Register 15
16E6	ACCDET_CON16	16	ACCDET Control Register 16
16EA	ACCDET_CON18	16	ACCDET Control Register 18
16F0	ACCDET_CON21	16	ACCDET Control Register 21
16F8	ACCDET_CON25	16	ACCDET Control Register 25
16FA	ACCDET_CON26	16	ACCDET Control Register 26
16FC	ACCDET_CON27	16	ACCDET Control Register 27

000A PONSTS Power On Source Record Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												STS_RBOOT	STS_SPAR	STS_CHRIN	STS_RTCA	STS_PWRKEY
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	STS_RBOOT	Power on for cold reset
3	STS_SPAR	Power on for SPAR event
2	STS_CHRIN	Power on for charger insertion
1	STS_RTCA	Power on for RTC alarm
0	STS_PWRKEY	Power on for PWREKY press

000C POFFSTS Power Off Source Record Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					STS_PUPSRC	STS_WDT	STS_DDLO	STS_BWDT	STS_NORMOFF	STS_PKEYLP	STS_CRST		STS_THRDN	STS_PSOC	STS_PGFAIL	STS_UVLO
Type					RO	RO	RO	RO	RO	RO	RO		RO	RO	RO	RO
Reset					0	0	0	0	0	0	0		0	0	0	0

Bit(s)	Name	Description
11	STS_PUPSRC	Power off for power source missing
10	STS_WDT	AP WDT
9	STS_DDLO	DDLO occurred after system on
8	STS_BWDT	Power off for BWDT
7	STS_NORMOFF	Power off for PWRHOLD clear
6	STS_PKEYLP	Power off for power key(s) long press
5	STS_CRST	Power off for cold reset
3	STS_THRDN	Power off for thermal shutdown
2	STS_PSOC	Power off for default on BUCK OC

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Bit(s)	Name	Description
1	STS_PGFAIL	Power off for PWRGOOD failure
0	STS_UVLO	Power off for UVLO event

000E **PSTSCTL** **Power On/Off Status Control** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_PONSTS_CLR								RG_POFFSTS_CLR
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
8	RG_PONSTS_CLR	Clears PONSTS
0	RG_POFFSTS_CLR	Clears POFFSTST and PG/OC status

0014 **PG_SDN_STS0** **Power Good Shutdown Status 0** **FFFF**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRUP_VS2_PG_STATUS	STRUP_VCORE_PG_STATUS	STRUP_VMODEM_PG_STATUS	STRUP_VS1_PG_STATUS	STRUP_VPROC_PG_STATUS		STRUP_VAUX18_PG_STATUS	STRUP_VSRAM_OTHERS_PG_STATUS	STRUP_VSRAM_GPU_PG_STATUS	STRUP_VA12_PG_STATUS	STRUP_VSRAM_PROC_PG_STATUS	STRUP_VIO18_PG_STATUS	STRUP_VEMC_PG_STATUS	STRUP_VIO28_PG_STATUS	STRUP_VDRAM_PG_STATUS	STRUP_VUSB_PG_STATUS
Type	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1		1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15	STRUP_VS2_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good
14	STRUP_VCORE_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good
13	STRUP_VMODEM_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good
12	STRUP_VS1_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good
11	STRUP_VPROC_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good
9	STRUP_VAUX18_P	**Shutdown PG status (cleared by SW)**

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Bit(s)	Name	Description
	G_STATUS	0: Power not good 1: Power good
8	STRUP_VSRAM_OTHERS_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good
7	STRUP_VSRAM_GPU_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good
6	STRUP_VA12_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good
5	STRUP_VSRAM_PROC_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good
4	STRUP_VIO18_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good
3	STRUP_VEMC_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good
2	STRUP_VIO28_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good
1	STRUP_VDRAM_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good
0	STRUP_VUSB_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good

0016 **PG_SDN_STS1** **Power Good Shutdown Status 1** **E000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRUP_VAUD28_PG_STATUS	STRUP_VXO22_PG_STATUS	STRUP_EXT_PMIC_PG_STATUS													
Type	RO	RO	RO													
Reset	1	1	1													

Bit(s)	Name	Description
15	STRUP_VAUD28_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good
14	STRUP_VXO22_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good

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Bit(s)	Name	Description
13	STRUP_EXT_PMIC_PG_STATUS	**Shutdown PG status (cleared by SW)** 0: Power not good 1: Power good

0018 OC_SDN_ST0 OC Shutdown Status 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRUP_VS2_OC_STATUS	STRUP_VCORE_OC_STATUS	STRUP_VMODEM_OC_STATUS	STRUP_VS1_OC_STATUS	STRUP_VPROC_OC_STATUS											
Type	RO	RO	RO	RO	RO											
Reset	0	0	0	0	0											

Bit(s)	Name	Description
15	STRUP_VS2_OC_STATUS	**Shutdown OC status (cleared by SW)** 0: No OC 1: OC occurs
14	STRUP_VCORE_OC_STATUS	**Shutdown OC status (cleared by SW)** 0: No OC 1: OC occurs
13	STRUP_VMODEM_OC_STATUS	**Shutdown OC status (cleared by SW)** 0: No OC 1: OC occurs
12	STRUP_VS1_OC_STATUS	**Shutdown OC status (cleared by SW)** 0: No OC 1: OC occurs
11	STRUP_VPROC_OC_STATUS	**Shutdown OC status (cleared by SW)** 0: No OC 1: OC occurs

0156 TOP_RST_MISC Reset Control Misc 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_PWRKEY_RST_TD								RG_WDTRSTB_DEB					RG_WDTRSTB_EN
Type			RW								RW					RW
Reset			0	0							0					0

Bit(s)	Name	Description
13:12	RG_PWRKEY_RST_TD	**Long pressed time to issue reset** 2'b00: 8 sec 2'b01: 11 sec

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Bit(s)	Name	Description
		2'b10: 14 sec 2'b11: 5 sec
5	RG_WDTRSTB_DEB	**Enables WDTRSTB debounce** 1'b0: No debounce 1'b1: Add debounce 1.6ms
0	RG_WDTRSTB_EN	**WDTRSTB(External Watchdog) reset from AP** 1'b0: Disable 1'b1: Enable

019C **TOP_INT_STATUS0** **TOP_INT_STATUS Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								INT_STATUS_MISC_TOP	INT_STATUS_AUD_TOP	INT_STATUS_XPP_TOP	INT_STATUS_HK_TOP	INT_STATUS_BM_TOP	INT_STATUS_SCK_TOP	INT_STATUS_PSC_TOP	INT_STATUS_LDO_TOP	INT_STATUS_BUCK_TOP
Type								RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	INT_STATUS_MISC_TOP	**Interrupt mask for TOP** 0: Unmask interrupt 1: Mask interrupt
7	INT_STATUS_AUD_TOP	**Interrupt mask for AUD** 0: Unmask interrupt 1: Mask interrupt
6	INT_STATUS_XPP_TOP	**Interrupt mask for XPP** 0: Unmask interrupt 1: Mask interrupt
5	INT_STATUS_HK_TOP	**Interrupt mask for HK** 0: Unmask interrupt 1: Mask interrupt
4	INT_STATUS_BM_TOP	**Interrupt mask for BM** 0: Unmask interrupt 1: Mask interrupt
3	INT_STATUS_SCK_TOP	**Interrupt mask for SCK** 0: Unmask interrupt 1: Mask interrupt
2	INT_STATUS_PSC_TOP	**Interrupt mask for LDO** 0: Unmask interrupt 1: Mask interrupt
1	INT_STATUS_LDO_TOP	**Interrupt mask for BUCK** 0: Unmask interrupt 1: Mask interrupt
0	INT_STATUS_BUCK_TOP	**Sets up TOP_INTM_CON0** 0: Unmask interrupt 1: Mask interrupt

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020C TOP_CLK_TRIM TOP_CLK_TRIM Register 70C0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_OSC_128K_TRIM														
Type		RO														
Reset		1	1	1	0	0	0									

Bit(s)	Name	Description
14:9	DA_OSC_128K_TRIM	128kHz OSC trimming bit

0294 RG_SPI_CON3 SPI Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RECORD_CMD0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RECORD_CMD0	

0296 RG_SPI_CON4 SPI Control Register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RECORD_CMD1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RECORD_CMD1	

0298 RG_SPI_CON5 SPI Control Register 5 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RECORD_CMD2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RECORD_CMD2	

029A RG_SPI_CON6 SPI Control Register 6 0000

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029A **RG_SPI_CON6** **SPI Control Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RECORD_WDATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RECORD_WDATA0	

029C **RG_SPI_CON7** **SPI Control Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RECORD_WDATA1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RECORD_WDATA1	

029E **RG_SPI_CON8** **SPI Control Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RECORD_WDATA2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RECORD_WDATA2	

02D8 **PSC_TOP_INT_STATUS0** **PSC_TOP INT Status Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_INT_STATUS_OV						RG_INT_STATUS_VCDT_HV_DET							
Type			RO						RO							
Reset			0						0							

Bit(s)	Name	Description
13	RG_INT_STATUS_	**OV interrupt status**

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Bit(s)	Name	Description
	OV	0: No interrupt issued 1: Interrupt issued
7	RG_INT_STATUS_VCDT_HV_DET	**VCDT_HV_DET interrupt status** 0: No interrupt issued 1: Interrupt issued

0308 STRUP_ANA_CON1 STRUP Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RGS_ANA_CHIP_ID															
Type	RO															
Reset	0	0	0													

Bit(s)	Name	Description
15:13	RGS_ANA_CHIP_ID	Chip ID

0346 PPCCTL0 PPC Control 0 Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_PWRHOLD
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_PWRHOLD	**Power hold** 0->1: Power hold 1->0: Power down

034C PPCCFG0 PPC Configuration 0 Register 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_WDTRST_ACT					
Type											RW					
Reset											0	0				

Bit(s)	Name	Description
5:4	RG_WDTRST_ACT	**PSEQ WDT actions** 00: PMIC reg reset 10: Cold reset

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0374 **STRUP_CON4** **STRUP DIG Control Register N4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		JUST_PWRKEY_RST	JUST_SMART_RST													
Type		RO	RO													
Reset		0	0													

Bit(s)	Name	Description
14	JUST_PWRKEY_RST	Long pressed reset indicator
13	JUST_SMART_RST	Smart reset indicator

0376 **STRUP_CON5** **STRUP DIG Control Register N5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DA_EXT_PMIC_EN2	DA_EXT_PMIC_EN1								
Type							RO	RO								
Reset							0	0								

Bit(s)	Name	Description
9	DA_EXT_PMIC_EN2	**External PMIC power on signal** 0: Shut down external PMIC 1: Power on external PMIC
8	DA_EXT_PMIC_EN1	**External PMIC power on signal** 0: Shut down external PMIC 1: Power on external PMIC

0384 **STRUP_CON12** **STRUP DIG Control Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_STRUP_LONG_PRESS_EXT_EN	RG_STRUP_LONG_PRESS_EXT_TD		RG_STRUP_LONG_PRESS_EXT_SEL	
Type												RW	RW		RW	
Reset												0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
4	RG_STRUP_LONG_PRESS_EXT_EN	**Enables re-power on scenario function** 1'b0: Disable long_press re-power on case 1'b1: Enable long_press re-power on case
3:2	RG_STRUP_LONG_PRESS_EXT_TD	**Selects delay time** 2'b00: 0.5s 2'b01: 1s 2'b10: 2s
1:0	RG_STRUP_LONG_PRESS_EXT_SEL	**Selects re-power on scenario** 2'b00: Debounce pwrkey 2'b01: After release pwrkey 2'b10: After release pwrkey and press pwrkey again

0386 **STRUP_CON13** **STRUP DIG Control Register 13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_STRUP_PWRKEY_COUNT_RESET
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_STRUP_PWRKEY_COUNT_RESET	**Resets long press shut-down counter** 1'b1: Reset long press counter 1'b0: Not reset long press counter

03C8 **CHR_TOP_CON0** **Charger Top Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RGS_CHRDET	RGS_CHR_LDO_DET			
Type												RO	RO			
Reset												0	0			

Bit(s)	Name	Description
4	RGS_CHRDET	**Detects charger-in** 0: No valid charger detected 1: Valid charger detected
3	RGS_CHR_LDO_DET	**Detects charger LDO** If not detected, VBUS detect function cannot work. 0: Invalid charger LDO 1: Valid charger LDO

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03CC **CHR_TOP_CON3** **Charger Top Control Register 3** 0009

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_UVLO_VTHL					RG_VCDT_UVLO_VTH	RG_VCDT_UVLO_EN
Type										RW					RW	RW
Reset										0	0	0	1	0	0	1

Bit(s)	Name	Description
6:2	RG_UVLO_VTHL	**Selects UVLO low threshold** 00000: 2.5V 00001: 2.55V 00010: 2.6V (default) 00011: 2.65V 00100: 2.7V 00101: 2.75V 00110: 2.8V 00111: 2.85V 01000: 2.9V
1	RG_VCDT_UVLO_VTH	**Selects VBUS_UVLO threshold** 0: 3.9V (default) 1: 3V
0	RG_VCDT_UVLO_EN	**Enables VBUS_UVLO threshold selection** 0: Disable 1: Enable (default)

03CE **CHR_TOP_CON4** **Charger Top Control Register 4** 0C4E

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VCDT_HV_VTH					RG_VCDT_LV_VTH					
Type						RW					RW					
Reset						1	0	0	0	1	0	0	1	1	1	

Bit(s)	Name	Description
10:6	RG_VCDT_HV_VTH	**ChargerIn LV detection threshold** Default: 4.3/10.5V for VTHL/VTHH 00010~01010: 4.0V,4.1V~4.45V with 50mV/step 01011~01110: 6V~7.5V with 500mV/step 01111~10011: 8.5 ~12.5 with 1000mV/step 10100: 14V
5:1	RG_VCDT_LV_VTH	**ChargerIn LV detection threshold** Default: 4.3/10.5V for VTHL/VTHH 00010~01010: 4.0V,4.1V~4.45V with 50mV/step 01011~01110: 6V~7.5V with 500mV/step 01111~10011: 8.5 ~12.5 with 1000mV/step 10100: 14V

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03D4 CHR_TOP_CON7 Charger Top Control Register 7 0083

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_LBAT_INT_VTH				
Type												RW				
Reset												0	0	0	1	1

Bit(s)	Name	Description
4:0	RG_LBAT_INT_VTH	**LBAT_INT threshold voltage** 00000: 2.5V 00001: 2.55V 00010: 2.6V 00011: 2.65V (default) 00100: 2.7V 00101: 2.75V 00110: 2.8V 00111: 2.85V 01000: 2.9V 01001: 2.95V 01010: 3.0V 01011: 3.05V 01100: 3.1V 01101: 3.15V 01110: 3.2V 01111: 3.25V 10000: 3.3V 10001: 3.35V 10010: 3.4V

0408 CHR_CON0 Charger Control Register 0 0F2F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCDT_HV_EN											
Type					RW											
Reset					1											

Bit(s)	Name	Description
11	RG_VCDT_HV_EN	**Enables ChargerIn HV detection function** 0: Disable 1: Enable

040C CHR_CON2 Charger Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RGS_VCDT_HV_DET	RGS_VCDT_LV_DET			
Type												RO	RO			

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Reset												0	0			

Bit(s)	Name	Description
4	RGS_VCDT_HV_DET	**Charger-in high voltage detection (with de-bounce)** 0: Charge-in voltage < VCDT_HV_VTH 1: Charge-in voltage > VCDT_HV_VTH
3	RGS_VCDT_LV_DET	**Charger-in low voltage detection (with de-bounce)** 0: Charge-in voltage < VCDT_LV_VTH 1: Charge-in voltage > VCDT_LV_VTH

0418 CHR_CON8 Charger Control Register 8 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RGS_BC11_CMP_OUT	RG_BC11_DCD_EN	RG_BC11_VSRC_EN		RG_BC11_RST	RG_BC11_BB_CTRL	RG_BC11_BIAS_EN	RG_BC11_IPU_EN		RG_BC11_IPD_EN		RG_BC11_CMP_EN		RG_BC11_VREF_VTH	
Type		RO	RW	RW		RW	RW	RW	RW		RW		RW		RW	
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	RGS_BC11_CMP_OUT	**Comparison result of BC12 charger detection** 0: DP or DM < BC12_VREF_VTH 1: DP or DM > BC12_VREF_VTH
13	RG_BC11_DCD_EN	**BC12 DCD connection check 15k resistor to gnd**
12:11	RG_BC11_VSRC_EN	**BC12 voltage source** Set VDP_SRC = 0.6V. 0: Disable voltage 1: Enable voltage source to DM 2: Enable voltage source to DP 3: Forbidden
10	RG_BC11_RST	**Resets BC12 detection mechanism in PCHR_DIG** 0: No effect 1: BC12 detection mechanism is disabled in PCHR_DIG.
9	RG_BC11_BB_CTRL	**Force BC12 charger detection controlled by baseband** 0: BC12 detection by PCHR_DIG (hardware mode) 1: BC12 detection by baseband (software mode)
8	RG_BC11_BIAS_EN	**Enables BC12 detection bias circuit** 0: Disable 1: Enable
7:6	RG_BC11_IPU_EN	**Enables BC12 7~15uA pull-up current** 0: Disable pull-up current 1: Enable pull-up current to DM 2: Enable pull-up current to DP 3: Forbidden
5:4	RG_BC11_IPD_EN	**BC12 50~150uA pull-down current** 0: Disable pull-down current 1: Enable pull-down current to DM 2: Enable pull-down current to DP 3: Enable pull-down current to DP and DM
3:2	RG_BC11_CMP_EN	**BC12 comparator connection** 0: Disable comparator 1: Enable comparator to DM

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Bit(s)	Name	Description
		2: Enable comparator to DP 3: Forbidden
1:0	RG_BC11_VREF_VTH	**VREF threshold voltage for comparator** 0: VREF_VTH=0.375V 1: VREF_VTH=1.2V 2,3: VREF_VTH=2.6V

042C **CHR_CON18** **Charger Control Register 18** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_ENVTEM_EN	RG_ENVTEM_D
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_ENVTEM_EN	**Blocks CHR_DET signal to start_up** 0: N/A 1: Enable write
0	RG_ENVTEM_D	**Blocks CHR_DET signal to start_up** 0: Not block 1: Block

0446 **BM_TOP_PAM0** **BM_TOP Parameter 0** **260A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BM_TOP_RST_OFFSET								BM_TOP_CLK_OFFSET							
Type	RU								RU							
Reset	0	0	1	0	0	1	1	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15:8	BM_TOP_RST_OFFSET	Reset setting offset
7:0	BM_TOP_CLK_OFFSET	Clock setting offset

0448 **BM_TOP_PAM1** **BM_TOP Parameter 1** **1232**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BM_TOP_INT_LEN								BM_TOP_INT_OFFSET							
Type	RU								RU							
Reset	0	0	0	1	0	0	1	0	0	0	1	1	0	0	1	0

Bit(s)	Name	Description
15:8	BM_TOP_INT_LEN	Interrupt setting length

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Bit(s)	Name	Description
7:0	BM_TOP_INT_OFFSET	Interrupt setting offset

044A **BM_TOP_CLK_CON0** **BM_TOP Clock Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_FGADC_32K_CK_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_FGADC_32K_CK_SEL	**Selects FGADC 32k clock source** 0: pmu_32k_ck 1: rtc_32k_ck

044C **BM_TOP_CKPDN_CON0** **BM_TOP_CKPDN Control Register 0** **F1E4**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_BM_TOP_CKPDN_CON0_RSV				RG_BM_INTRP_PRE_OC_CK_PDN	RG_BM_INTRP_CK_PDN	RG_PMU26M_CK_DIV_PDN	RG_BIF_X104_CK_PDN	RG_BIF_X4_CK_PDN	RG_BIF_X1_CK_PDN	RG_G_BIF_1M_CK_PDN	RG_FGADC_ANA_CK_PDN	RG_FGADC_DIG_CK_PDN	RG_FGADC_FT_CK_PDN	RG_BATON_1K_CK_PDN	RG_BATON_32K_CK_PDN
Type	RW				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	0	0	0	1	1	1	1	0	0	1	0	0

Bit(s)	Name	Description
15:12	RG_BM_TOP_CKPDN_CON0_RSV	**Powers down BM_TOP_CKPDN_CON0** 0: Power on 1: Power down
11	RG_BM_INTRP_PRE_OC_CK_PDN	**Powers down BM_INTRP_PRE_OC_CK** 0: Power on 1: Power down
10	RG_BM_INTRP_CK_PDN	**Powers down BM_INTRP_CK** 0: Power on 1: Power down
9	RG_PMU26M_CK_DIV_PDN	**Powers down PMU26M_CK_DIV** 0: Power on 1: Power down
8	RG_BIF_X104_CK_	**Powers down BIF_X104_CK**

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Bit(s)	Name	Description
	PDN	0: Power on 1: Power down
7	RG_BIF_X4_CK_PDN	**Powers down BIF_X4_CK** 0: Power on 1: Power down
6	RG_BIF_X1_CK_PDN	**Powers down BIF_X1_CK** 0: Power on 1: Power down
5	RG_G_BIF_1M_CK_PDN	**Powers down G_BIF_1M_CK** 0: Power on 1: Power down
4	RG_FGADC_ANA_CK_PDN	**Powers down FGADC_ANA_CK** 0: Power on 1: Power down
3	RG_FGADC_DIG_CK_PDN	**Powers down FGADC_DIG_CK** 0: Power on 1: Power down
2	RG_FGADC_FT_CK_PDN	**Powers down FGADC_FT_CK** 0: Power on 1: Power down
1	RG_BATON_1K_CK_PDN	**Powers down BATON_1K_CK** 0: Power on 1: Power down
0	RG_BATON_32K_CK_PDN	**Powers down BATON_32K_CK** 0: Power on 1: Power down

044E **BM_TOP_CKPDN_CON0_SET** **BM_TOP_CKPDN_CON0 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BM_TOP_CKPDN_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BM_TOP_CKPDN_CON0_SET	**Sets up BM_TOP_CKPDN_CON0** 1'b0: Not set 1'b1: Set

0450 **BM_TOP_CKPDN_CON0_CLR** **BM_TOP_CKPDN_CON0 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BM_TOP_CKPDN_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	BM_TOP_CKPDN_CON0_CLR	**Clears BM_TOP_CKPDN_CON0** 1'b0: Not clear 1'b1: Clear

0452 BM_TOP_CKSEL_CON0 — BM_TOP_CKSEL Control Register 0 — 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_BM_TOP_CKSEL_CON0_RSV															RG_FGADC_ANA_CK_CKSEL
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:1	RG_BM_TOP_CKSEL_CON0_RSV	**Selects TOP clock**
0	RG_FGADC_ANA_CK_CKSEL	**Selects FGADC_ANA_CK clock** 1'b0: rtc_32k_ck 1'b1: FGADC_FT_CK_DIV8

0454 BM_TOP_CKSEL_CON0_SET — BM_TOP_CKSEL_CON0 Register SET — 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BM_TOP_CKSEL_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BM_TOP_CKSEL_CON0_SET	**Sets up BM_TOP_CKSEL_CON0** 1'b0: Not set 1'b1: Set

0456 BM_TOP_CKSEL_CON0_CLR — BM_TOP_CKSEL_CON0 Register CLR — 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BM_TOP_CKSEL_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:0	BM_TOP_CKSEL_CON0_CLR	**Clears BM_TOP_CKSEL_CON0** 1'b0: Not clear 1'b1: Clear

0458 **BM_TOP_CKDIVSEL_CON0** **BM_TOP_CKDIVSEL Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BM_TOP_CKDIVSEL_CON0_RSV													RG_BIF_X4_CK_DIVSEL		
Type	RW													RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:3	BM_TOP_CKDIVSEL_CON0_RSV	
2:0	RG_BIF_X4_CK_DIVSEL	**Selects BIF_X4_CK divider** 3'b000: DIV1 3'b001: DIV2 3'b010: DIV4 3'b011: DIV8 3'b1xx: DIV16

045A **BM_TOP_CKDIVSEL_CON0_SET** **BM_TOP_CKDIVSEL_CON0 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BM_TOP_CKDIVSEL_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BM_TOP_CKDIVSEL_CON0_SET	**Sets up BM_TOP_CKDIVSEL_CON0** 1'b0: Not set 1'b1: Set

045C **BM_TOP_CKDIVSEL_CON0_CLR** **BM_TOP_CKDIVSEL_CON0 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BM_TOP_CKDIVSEL_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BM_TOP_CKDIVSE	**Clears BM_TOP_CKDIVSEL_CON0**

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Bit(s)	Name	Description
	L_CON0_CLR	1'b0: Not clear 1'b1: Clear

045E	BM_TOP_CKHWEN_CON0	BM_TOP_CKHWEN Control Register 0	0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BIF_X104_CK_PDN_HWEN	RG_BIF_X4_CK_PDN_HWEN
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
1	RG_BIF_X104_CK_PDN_HWEN	**BIF_X104_CK power down control** 0: SW mode 1: HW mode
0	RG_BIF_X4_CK_PDN_HWEN	**BIF_X4_CK power down control** 0: SW mode 1: HW mode

0460	BM_TOP_CKHWEN_CON0_SET	BM_TOP_CKHWEN_CON0 Register SET	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BM_TOP_CKHWEN_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BM_TOP_CKHWEN_CON0_SET	**Sets up BM_TOP_CKHWEN_CON0** 1'b0: Not set 1'b1: Set

0462	BM_TOP_CKHWEN_CON0_CLR	BM_TOP_CKHWEN_CON0 Register CLR	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BM_TOP_CKHWEN_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:0	BM_TOP_CKHWEN_CON0_CLR	**Clears BM_TOP_CKHWEN_CON0** 1'b0: Not clear 1'b1: Clear

0514 **FGADC_CUR_CON0** **FGADC_CUR Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CURRENT_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CURRENT_OUT	Current output charge of first stage [15:0]

051C **FGADC_CAR_CON0** **FGADC_CAR Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CAR_31_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CAR_31_16	Current charge value [31:16]

051E **FGADC_CAR_CON1** **FGADC_CAR Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CAR_15_00															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CAR_15_00	Current charge value [15:0]

0530 **FGADC_NCAR_CON0** **FGADC_NCAR Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_NCAR_31_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	FG_NCAR_31_16	Current n_charge value [31:16]

0532 **FGADC_NCAR_CON1** **FGADC_NCAR Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_NCAR_15_00															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_NCAR_15_00	Current n_charge value [15:0]

0538 **FGADC_IAVG_CON0** **FGADC_IAVG Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_IAVG_VLD				FG_IAVG_27_16											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	FG_IAVG_VLD	**FGADC average current valid** 1'b0: Invalid 1'b1: Valid
11:0	FG_IAVG_27_16	**Current FGADC average current [27:16]**

053A **FGADC_IAVG_CON1** **FGADC_IAVG Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_IAVG_15_00															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_IAVG_15_00	**Current FGADC average current [15:0]** Unit of FG_IAVG is [LSB of charge/32]

0544 **FGADC_NTER_CON0** **FGADC_NTER Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			FG_NTER_29_16													

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Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	FG_NTER_29_16	Current charge time value [29:16]

0546 FGADC_NTER_CON1 FGADC_NTER Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_NTER_15_00															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_NTER_15_00	Current charge time value [15:0]

0606 BATON_ANA_CON0 BATON Analog Control Register 0 0005

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RGS_BATON_UNDET	
Type															RO	
Reset															0	

Bit(s)	Name	Description
1	RGS_BATON_UNDET	**Battery-on undetected** 0: Detected 1: Not detected

0686 BIF_CON0 BIF Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_0										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_0	Command queue 0

0688 BIF_CON1 BIF Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_1										
Type						RW										

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Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_1	Command queue 1

068A **BIF_CON2** **BIF Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_2										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_2	Command queue 2

068C **BIF_CON3** **BIF Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_3										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_3	Command queue 3

068E **BIF_CON4** **BIF Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_4										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_4	Command queue 4

0690 **BIF_CON5** **BIF Control Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_5										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_5	Command queue 5

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0692 **BIF_CON6** **BIF Control Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_6										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_6	Command queue 6

0694 **BIF_CON7** **BIF Control Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_7										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_7	Command queue 7

0696 **BIF_CON8** **BIF Control Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_8										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_8	Command queue 8

0698 **BIF_CON9** **BIF Control Register 9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_9										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_9	Command queue 9

069A **BIF_CON10** **BIF Control Register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_10										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
10:0	BIF_COMMAND_10	Command queue 10

069C **BIF_CON11** **BIF Control Register 11** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_11										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_11	Command queue 11

069E **BIF_CON12** **BIF Control Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_12										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_12	Command queue 12

06A0 **BIF_CON13** **BIF Control Register 13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_13										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_13	Command queue 13

06A2 **BIF_CON14** **BIF Control Register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_14										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_14	Command queue 14

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06A4 **BIF_CON15** **BIF Control Register 15** **4000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_TRASFER_NUM						BIF_COMMAND_TYPE									
Type	RW						RW									
Reset	0	1	0	0			0	0								

Bit(s)	Name	Description
15:12	BIF_TRASFER_NUM	**Total transfer number in command queue**
9:8	BIF_COMMAND_TYPE	**Command type** 2'b00: Write 2'b01: Read data 2'b10: Read response

06A6 **BIF_CON16** **BIF Control Register 16** **1431**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_STOP_SET							BIF_LOGIC_1_SET					BIF_LOGIC_0_SET			
Type	RW							RW					RW			
Reset	0	0	0	1	0	1		0	0	0	1	1	0	0	0	1

Bit(s)	Name	Description
15:10	BIF_STOP_SET	**Sets up stop signal spec** 6'd0: 0T 6'd1: 1T 6'd2: 2T 6'dN: NT
8:4	BIF_LOGIC_1_SET	**Sets up logic "1" period spec** 5'd0: 0T 5'd1: 1T 5'd2: 2T 5'dN: NT
3:0	BIF_LOGIC_0_SET	**Sets up logic "0" period spec** 4'd0: 0T 4'd1: 1T 4'd2: 2T 4'dN: NT

06A8 **BIF_CON17** **BIF Control Register 17** **1010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_READ_EXPECT_NUM											BIF_DEBOUNCE_EN				
Type	RW											RW				
Reset	0	0	0	1								1				

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Bit(s)	Name	Description
15:12	BIF_READ_EXPECT_NUM	**Expected number of read back data** 0: 0 1: 1 data package
4	BIF_DEBOUNCE_EN	**No function** 1'b0: Disable 1'b1: Enable

06AA **BIF_CON18** **BIF Control Register 18** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BIF_TRASACT_TRIGGER
Type																RW
Reset																0

Bit(s)	Name	Description
0	BIF_TRASACT_TRIGGER	**Trigger signal** 1'b1: Trigger BIF module

06AC **BIF_CON19** **BIF Control Register 19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BIF_RESPONSE									BIF_DATA_NUM			
Type				RO									RO			
Reset				0									0	0	0	0

Bit(s)	Name	Description
12	BIF_RESPONSE	**Response result** 1'b0: Negative response 1'b1: Positive response
3:0	BIF_DATA_NUM	**Number of read back data**

06AE **BIF_CON20** **BIF Control Register 20** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_0							BIF_ACK_0	BIF_DATA_0							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	BIF_ERROR_0	**Error happens or not** 1'b0: No error 1'b1: Error exists
8	BIF_ACK_0	
7:0	BIF_DATA_0	**Read back data**

06B0 **BIF_CON21** **BIF Control Register 21** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_1							BIF_ACK_1	BIF_DATA_1							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_1	**Error happens or not** 1'b0: No error 1'b1: Error exists
8	BIF_ACK_1	
7:0	BIF_DATA_1	**Read back data**

06B2 **BIF_CON22** **BIF Control Register 22** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_2							BIF_ACK_2	BIF_DATA_2							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_2	**Error happens or not** 1'b0: No error 1'b1: Error exists
8	BIF_ACK_2	
7:0	BIF_DATA_2	**Read back data**

06B4 **BIF_CON23** **BIF Control Register 23** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_3							BIF_ACK_3	BIF_DATA_3							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	BIF_ERROR_3	**Error happens or not** 1'b0: No error 1'b1: Error exists
8	BIF_ACK_3	
7:0	BIF_DATA_3	**Read back data**

06B6 **BIF_CON24** **BIF Control Register 24** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_4							BIF_ACK_4	BIF_DATA_4							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_4	**Error happens or not** 1'b0: No error 1'b1: Error exists
8	BIF_ACK_4	
7:0	BIF_DATA_4	**Read back data**

06B8 **BIF_CON25** **BIF Control Register 25** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_5							BIF_ACK_5	BIF_DATA_5							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_5	**Error happens or not** 1'b0: No error 1'b1: Error exists
8	BIF_ACK_5	
7:0	BIF_DATA_5	**Read back data**

06BA **BIF_CON26** **BIF Control Register 26** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_6							BIF_ACK_6	BIF_DATA_6							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	BIF_ERROR_6	**Error happens or not** 1'b0: No error 1'b1: Error exists
8	BIF_ACK_6	
7:0	BIF_DATA_6	**Read back data**

06BC **BIF_CON27** **BIF Control Register 27** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_7							BIF_ACK_7	BIF_DATA_7							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_7	**Error happens or not** 1'b0: No error 1'b1: Error exists
8	BIF_ACK_7	
7:0	BIF_DATA_7	**Read back data**

06BE **BIF_CON28** **BIF Control Register 28** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_8							BIF_ACK_8	BIF_DATA_8							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_8	**Error happens or not** 1'b0: No error 1'b1: Error exists
8	BIF_ACK_8	
7:0	BIF_DATA_8	**Read back data**

06C0 **BIF_CON29** **BIF Control Register 29** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_9							BIF_ACK_9	BIF_DATA_9							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	BIF_ERROR_9	**Error happens or not** 1'b0: No error 1'b1: Error exists
8	BIF_ACK_9	
7:0	BIF_DATA_9	**Read back data**

06C4 BIF_CON31 BIF Control Register 31 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_BUS_STATUS	BIF_TOTAL_VALID	BIF_BAT_UNDET	BIF_TIMEOUT	BIF_IRQ										BIF_IRQ_CLR	BIF_BACK_NORMAL
Type	RO	RO	RO	RO	RO										RW	RW
Reset	0	0	0	0	0										0	0

Bit(s)	Name	Description
15	BIF_BUS_STATUS	**Busy: BIF is still in action** 1'b0: Complete 1'b1: Busy
14	BIF_TOTAL_VALID	**Error happens or not in all read data** 1'b0: No error 1'b1: Error exists (for all data)
13	BIF_BAT_UNDET	**Battery status** 1'b0: Battery exists 1'b1: Battery undetected
12	BIF_TIMEOUT	**Timeout status** 1'b1: Timeout
11	BIF_IRQ	**BIF interrupt status** Because this register is cleared by the hardware, the interrupt edge-sensitive scheme should be adopted for this design. 1'b1: Interrupt issue
1	BIF_IRQ_CLR	**Clears BIF interrupt status** When BIF interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status.
0	BIF_BACK_NORMAL	**Finishes interrupt mode** 1'b1: Abort interrupt mode

06C6 BIF_CON32 BIF Control Register 32 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_POWER_UP											BIF_POWER_UP_COUNT				
Type	RW											RW				
Reset	0											1	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	BIF_POWER_UP	**Power up trigger** 1'b1: Power up slave device
4:0	BIF_POWER_UP_COUNT	**Power up counter setting** 5'd0: 0 5'd1: 1T 5'd2: 2T 5'dN: NT

06D0 BIF_CON37 BIF Control Register 37 000B

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_TIMEOUT_SET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

Bit(s)	Name	Description
15:0	BIF_TIMEOUT_SET	**Sets up RX timeout threshold** 16'd0: 0T 16'd1: 1T 16'd2: 2T 16'dN: NT

06D2 BIF_CON38 BIF Control Register 38 8031

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_RX_DEG_EN					BIF_RX_DEG_WND										
Type	RW					RW										
Reset	1					0	0	0	0	0	1	1	0	0	0	1

Bit(s)	Name	Description
15	BIF_RX_DEG_EN	**Enables deglitch function** 1'b0: Bypass 1'b1: Enable HW deglitch function
10:0	BIF_RX_DEG_WND	**Filter window** 10'd0: 1T 10'd1: 2T 10'd2: 3T 10'dN: (N+1)T

0786 AUXADC_ADC0 AUXADC ADC Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_	AUXADC_ADC_OUT_CH0														

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	CH0															
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0	**AUXADC channel 0 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0	**AUXADC channel 0 output data**

0788 **AUXADC_ADC1** **AUXADC ADC Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1	AUXADC_ADC_OUT_CH1														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1	**AUXADC channel 1 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1	**AUXADC channel 1 output data**

078A **AUXADC_ADC2** **AUXADC ADC Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH2				AUXADC_ADC_OUT_CH2											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH2	**AUXADC channel 2 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH2	**AUXADC channel 2 output data**

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078C	AUXADC_ADC3	AUXADC ADC Register 3	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH3				AUXADC_ADC_OUT_CH3											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH3	**AUXADC channel 3 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH3	**AUXADC channel 3 output data**

078E	AUXADC_ADC4	AUXADC ADC Register 4	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4				AUXADC_ADC_OUT_CH4											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4	**AUXADC channel 4 output data**

0790	AUXADC_ADC5	AUXADC ADC Register 5	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH5				AUXADC_ADC_OUT_CH5											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RD	**AUXADC channel 5 output data ready**

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Bit(s)	Name	Description
	Y_CH5	0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH5	**AUXADC channel 5 output data**

0792 **AUXADC_ADC6** **AUXADC ADC Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH6				AUXADC_ADC_OUT_CH6											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH6	**AUXADC channel 6 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH6	**AUXADC channel 6 output data**

0794 **AUXADC_ADC7** **AUXADC ADC Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7	AUXADC_ADC_OUT_CH7														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7	**AUXADC channel 7 output data**

0796 **AUXADC_ADC8** **AUXADC ADC Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC				AUXADC_ADC_OUT_CH8											

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	_ADC_RDY_CH8															
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH8	**AUXADC channel 8 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH8	**AUXADC channel 8 output data**

0798 **AUXADC_ADC9** **AUXADC ADC Register 9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH9	AUXADC_ADC_OUT_CH9														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH9	**AUXADC channel 9 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH9	**AUXADC channel 9 output data**

079A **AUXADC_ADC10** **AUXADC ADC Register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH10				AUXADC_ADC_OUT_CH10											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH10	**AUXADC channel 10 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH10	**AUXADC channel 10 output data**

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079C	AUXADC_ADC11	AUXADC ADC Register 11	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH11				AUXADC_ADC_OUT_CH11											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH11	**AUXADC channel 11 output data ready (used for BIF)** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH11	**AUXADC channel 11 output data (used for BIF)**

079E	AUXADC_ADC12	AUXADC ADC Register 12	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH12_15	AUXADC_ADC_OUT_CH12_15														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH12_15	**AUXADC channel 12_15 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH12_15	**AUXADC channel 12_15 output data**

07A0	AUXADC_ADC13	AUXADC ADC Register 13	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_THR_HW				AUXADC_ADC_OUT_THR_HW											

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Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_THR_HW	**AUXADC channel 4 output data ready (for pmic_temp)** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_THR_HW	**AUXADC channel 4 output data**

07A2 **AUXADC_ADC14** **AUXADC ADC Register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_LBAT**				**AUXADC_ADC_OUT_LBAT**											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_LBAT	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_LBAT	**AUXADC low battery output data**

07A4 **AUXADC_ADC15** **AUXADC ADC Register 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_LBAT2**				**AUXADC_ADC_OUT_LBAT2**											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_LBAT2	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_LBAT2	**AUXADC low battery output data**

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07A6 **AUXADC_ADC16** **AUXADC ADC Register 16** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_BY_GPS	AUXADC_ADC_OUT_CH7_BY_GPS														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_GPS	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_GPS	**AUXADC channel 7 output data**

07A8 **AUXADC_ADC17** **AUXADC ADC Register 17** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_BY_MD	AUXADC_ADC_OUT_CH7_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_MD	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_MD	**AUXADC channel 7 output data**

07AA **AUXADC_ADC18** **AUXADC ADC Register 18** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_BY_AP	AUXADC_ADC_OUT_CH7_BY_AP														

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Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_AP	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_AP	**AUXADC channel 7 output data**

07AC **AUXADC_ADC19** **AUXADC ADC Register 19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_CH4_BY_MD**				**AUXADC_ADC_OUT_CH4_BY_MD**											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4_BY_MD	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4_BY_MD	**AUXADC channel 4 output data**

07AE **AUXADC_ADC20** **AUXADC ADC Register 20** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_PWRON_PCHR**	**AUXADC_ADC_OUT_PWRON_PCHR**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_PWRON_PCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_PWRON_PCHR	**AUXADC wakeup output data**

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07B0 AUXADC_ADC21 AUXADC ADC Register 21 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_PWRON_SWCHR	AUXADC_ADC_OUT_PWRON_SWCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_PWRON_SWCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_PWRON_SWCHR	**AUXADC wakeup output data**

07B2 AUXADC_ADC22 AUXADC ADC Register 22 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_WAKEUP_PCHR	AUXADC_ADC_OUT_WAKEUP_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_WAKEUP_PCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_WAKEUP_PCHR	**AUXADC wakeup output data**

07B4 AUXADC_ADC23 AUXADC ADC Register 23 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC	AUXADC_ADC_OUT_WAKEUP_SWCHR														

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	_ADC_RDY_WAKEUP_SWCHR															
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_WAKEUP_SWCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_WAKEUP_SWCHR	**AUXADC wakeup output data**

07B6 AUXADC_ADC24 AUXADC ADC Register 24 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0_BY_MD	AUXADC_ADC_OUT_CH0_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0_BY_MD	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0_BY_MD	**AUXADC channel output data**

07B8 AUXADC_ADC25 AUXADC ADC Register 25 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0_BY_AP	AUXADC_ADC_OUT_CH0_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0_BY_AP	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0_BY_AP	**AUXADC channel output data**

07BA **AUXADC_ADC26** AUXADC ADC Register 26 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1_BY_MD	AUXADC_ADC_OUT_CH1_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1_BY_MD	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1_BY_MD	**AUXADC channel output data**

07BC **AUXADC_ADC27** AUXADC ADC Register 27 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1_BY_AP	AUXADC_ADC_OUT_CH1_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1_BY_AP	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1_BY_AP	**AUXADC channel output data**

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07BE **AUXADC_ADC28** **AUXADC ADC Register 28** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_BAT_TEMP				AUXADC_ADC_OUT_BAT_TEMP											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_BAT_TEMP	**AUXADC BAT_TEMP output data ready** 0: AUXADC BAT_TEMP data proceeding 1: AUXADC BAT_TEMP data ready
11:0	AUXADC_ADC_OUT_BAT_TEMP	**AUXADC BAT_TEMP output data**

07C0 **AUXADC_ADC29** **AUXADC ADC Register 29** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_FGADC_PCHR	AUXADC_ADC_OUT_FGADC_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_FGADC_PCHR	**AUXADC output data ready (BATSNS)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_FGADC_PCHR	**AUXADC output data**

07C2 **AUXADC_ADC30** **AUXADC ADC Register 30** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_FGADC_SWC	AUXADC_ADC_OUT_FGADC_SWCHR														

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	HR															
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_FGADC_SWCHR	**AUXADC output data ready (ISENSE)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_FGADC_SWCHR	**AUXADC output data**

07C4 AUXADC_ADC31 AUXADC ADC Register 31 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_BAT_PLUGIN_PCHR	AUXADC_ADC_OUT_BAT_PLUGIN_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_BAT_PLUGIN_PCHR	**AUXADC output data ready (BATSNS)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_BAT_PLUGIN_PCHR	**AUXADC output data**

07C6 AUXADC_ADC32 AUXADC ADC Register 32 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_BAT_PLUGIN_SWCHR	AUXADC_ADC_OUT_BAT_PLUGIN_SWCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	AUXADC_ADC_RDY_BAT_PLUGIN_SWCHR	**AUXADC output data ready (ISENSE)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_BAT_PLUGIN_SWCHR	**AUXADC output data**

07C8 AUXADC_ADC33 AUXADC ADC Register 33 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_IMP	AUXADC_ADC_OUT_IMP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_IMP	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_IMP	**AUXADC output data**

07CA AUXADC_ADC34 AUXADC ADC Register 34 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_IMP_AVG	AUXADC_ADC_OUT_IMP_AVG														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_IMP_AVG	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_IMP_AVG	**AUXADC output data**

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07CC **AUXADC_ADC35** **AUXADC ADC Register 35** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AUXADC_ADC_OUT_RAW														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:0	AUXADC_ADC_OUT_RAW	AUXADC channel output raw data

07CE **AUXADC_ADC36** **AUXADC ADC Register 36** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_MDRT	AUXADC_ADC_OUT_MDRT														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_MDRT	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_MDRT	**AUXADC output data**

07D0 **AUXADC_ADC37** **AUXADC ADC Register 37** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_JEITA				AUXADC_ADC_OUT_JEITA											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_JEITA	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_JEITA	**AUXADC output data**

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07DA AUXADC_ADC42 AUXADC ADC Register 42 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_NAG	AUXADC_ADC_OUT_NAG														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_NAG	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_NAG	**AUXADC output data**

07DC AUXADC_ADC43 AUXADC ADC Register 43 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_BATID				AUXADC_ADC_OUT_BATID											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_BATID	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_BATID	**AUXADC output data**

07E2 AUXADC_ADC46 AUXADC ADC Register 46 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4_BY_THR1				AUXADC_ADC_OUT_CH4_BY_THR1											
Type	RO				RO											

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Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4_BY_THR1	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4_BY_THR1	**AUXADC channel 4 output data**

07E4 AUXADC_ADC47 AUXADC ADC Register 47 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4_BY_THR2				AUXADC_ADC_OUT_CH4_BY_THR2											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4_BY_THR2	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4_BY_THR2	**AUXADC channel 4 output data**

07E6 AUXADC_STA0 AUXADC_STA0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_BUSY_IN_WAKEUP	AUXADC_ADC_BUSY_IN_BAT_TEMP	AUXADC_ADC_BUSY_IN_LBAT2	AUXADC_ADC_BUSY_IN_LBAT	AUXADC_ADC_BUSY_IN											
Type	RO	RO	RO	RO	RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_WAKEUP	**ADC busy status** 0: IDLE 1: BUSY
14	AUXADC_ADC_BUSY_IN_BAT_TEMP	**ADC busy status** 0: IDLE

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Bit(s)	Name	Description
		1: BUSY
13	AUXADC_ADC_BUSY_IN_LBAT2	**ADC busy status** 0: IDLE 1: BUSY
12	AUXADC_ADC_BUSY_IN_LBAT	**ADC busy status** 0: IDLE 1: BUSY
11:0	AUXADC_ADC_BUSY_IN	**AUXADC ADC BUSY status** bit[11] = CH11 ~ bit[0] = CH0 0: IDLE 1: BUSY

07E8 **AUXADC_STA1** **AUXADC_STA1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_BUSY_IN_THR_MD	AUXADC_ADC_BUSY_IN_THR_HW	AUXADC_ADC_BUSY_IN_GPS	AUXADC_ADC_BUSY_IN_GPS_MD	AUXADC_ADC_BUSY_IN_GPS_AP	AUXADC_ADC_BUSY_IN_FGADC_SWCHR	AUXADC_ADC_BUSY_IN_FGADC_PCHR	AUXADC_ADC_BUSY_IN_IMP	AUXADC_ADC_BUSY_IN_SHARE		AUXADC_ADC_BUSY_IN_MDRT	AUXADC_ADC_BUSY_IN_JEITA				
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO		RO	RO				
Reset	0	0	0	0	0	0	0	0	0		0	0				

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_THR_MD	**ADC busy status** 0: IDLE 1: BUSY
14	AUXADC_ADC_BUSY_IN_THR_HW	**ADC busy status** 0: IDLE 1: BUSY
13	AUXADC_ADC_BUSY_IN_GPS	**ADC busy status** 0: IDLE 1: BUSY
12	AUXADC_ADC_BUSY_IN_GPS_MD	**ADC busy status** 0: IDLE 1: BUSY
11	AUXADC_ADC_BUSY_IN_GPS_AP	**ADC busy status** 0: IDLE 1: BUSY
10	AUXADC_ADC_BUSY_IN_FGADC_SWCHR	**ADC busy status** 0: IDLE 1: BUSY
9	AUXADC_ADC_BUSY_IN_FGADC_PCHR	**ADC busy status** 0: IDLE 1: BUSY
8	AUXADC_ADC_BUSY_IN_IMP	**ADC busy status** 0: IDLE

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Bit(s)	Name	Description
		1: BUSY
7	AUXADC_ADC_BUSY_IN_SHARE	**ADC busy status** 0: IDLE 1: BUSY
5	AUXADC_ADC_BUSY_IN_MDRT	**ADC busy status** 0: IDLE 1: BUSY
4	AUXADC_ADC_BUSY_IN_JEITA	**ADC busy status** 0: IDLE 1: BUSY

07EA **AUXADC_STA2** **AUXADC_STA2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_BUSY_IN_NAG**			**AUXADC_ADC_BUSY_IN_THR2**	**AUXADC_ADC_BUSY_IN_THR1**								**AUXADC_ADC_BUSY_IN_PWRON**	**AUXADC_ADC_BUSY_IN_BATID**	**AUXADC_ADC_BUSY_IN_BAT_PLUGIN_SWCHR**	**AUXADC_ADC_BUSY_IN_BAT_PLUGIN_PCHR**
Type	RO	RO	RO	RO	RO								RO	RO	RO	RO
Reset	0	0	0	0	0								0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_NAG	**ADC busy status** 0: IDLE 1: BUSY
12	AUXADC_ADC_BUSY_IN_THR2	**ADC busy status** 0: IDLE 1: BUSY
11	AUXADC_ADC_BUSY_IN_THR1	**ADC busy status** 0: IDLE 1: BUSY
3	AUXADC_ADC_BUSY_IN_PWRON	**ADC busy status** 0: IDLE 1: BUSY
2	AUXADC_ADC_BUSY_IN_BATID	**ADC busy status** 0: IDLE 1: BUSY
1	AUXADC_ADC_BUSY_IN_BAT_PLUGIN_SWCHR	**ADC busy status** 0: IDLE 1: BUSY
0	AUXADC_ADC_BUSY_IN_BAT_PLUGIN_PCHR	**ADC busy status** 0: IDLE 1: BUSY

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0992	SCK_TOP_CKPDN_CON0	SCK_CKPDN Control Register 0	004B

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_RTC_2SEC_OFF_DET_PDN	RG_RTC_26M_CK_PDN	RG_RTC_32K_CK_PDN	RG_RTC_MCLK_PDN	RG_RTC_SEC_32K_CK_PDN	RG_RTC_EOSC32_CK_PDN	RG_EOSC_CALI_TEST_CK_PDN	RG_RTC_SEC_MCLK_PDN
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	1	0	0	1	0	1	1

Bit(s)	Name	Description
7	RG_RTC_2SEC_OFF_DET_PDN	**Powers down RTC_2SEC_OFF_DET** 0: Power on 1: Power down
6	RG_RTC_26M_CK_PDN	**Powers down RTC_26M_CK** 0: Power on 1: Power down
5	RG_RTC_32K_CK_PDN	**Powers down RTC_32K_CK** 0: Power on 1: Power down
4	RG_RTC_MCLK_PDN	**Powers down RTC_MCLK** 0: Power on 1: Power down
3	RG_RTC_SEC_32K_CK_PDN	**Powers down RTC_SEC_32K_CK** 0: Power on 1: Power down
2	RG_RTC_EOSC32_CK_PDN	**Powers down RTC_EOSC32_CK** 0: Power on 1: Power down
1	RG_EOSC_CALI_TEST_CK_PDN	**Powers down EOSC_CALI_TEST_CK** 0: Power on 1: Power down
0	RG_RTC_SEC_MCLK_PDN	**Powers down RTC_SEC_MCLK** 0: Power on 1: Power down

0994	SCK_TOP_CKPDN_CON0_SET	SCK_CKPDN Control Register 0 SET	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SCK_TOP_CKPDN_CON0_SET							
Type									W1							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SCK_TOP_CKPDN_	**Sets up SCK_TOP_CKPDN_CON0**

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Bit(s)	Name	Description
	CON0_SET	1'b0: Not set 1'b1: Set

0996 **SCK_TOP_CKPDN_CON0_CLR** **SCK_CKPDN Control Register 0 CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SCK_TOP_CKPDN_CON0_CLR							
Type									W1							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SCK_TOP_CKPDN_CON0_CLR	**Clears SCK_TOP_CKPDN_CON0** 1'b0: Not clear 1'b1: Clear

0998 **SCK_TOP_CKHWEN_CON0** **SCK_CKHWEN Control Register 0** **03F1**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_RTC_CLK_PDN_HWEN_RSV_0						RG_RTC_CLK_PDN_HWEN_RSV_1						RG_RTC_SEC_MCLK_PDN_HWEN	RG_RTC_SEC_32K_CK_PDN_HWEN	RG_RTC_MCLK_PDN_HWEN	RG_RTC_26M_CK_PDN_HWEN
Type	RW						RW						RW	RW	RW	RW
Reset	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	1

Bit(s)	Name	Description
15:10	RG_RTC_CLK_PDN_HWEN_RSV_0	**RESERVED_0** 0: SW mode 1: HW mode
9:4	RG_RTC_CLK_PDN_HWEN_RSV_1	**RESERVED_1** 0: SW mode 1: HW mode
3	RG_RTC_SEC_MCLK_PDN_HWEN	**RTC_SEC_MCLK power down control** 0: SW mode 1: HW mode
2	RG_RTC_SEC_32K_CK_PDN_HWEN	**RTC_SEC_32K_CK power down control** 0: SW mode 1: HW mode
1	RG_RTC_MCLK_PDN_HWEN	**RTC_MCLK power down control** 0: SW mode 1: HW mode
0	RG_RTC_26M_CK	**RTC_26M_CK power down control**

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Bit(s)	Name	Description
	_PDN_HWEN	0: SW mode 1: HW mode

099A **SCK_TOP_CKHWEN_CON0_SET** **SCK_CKHWEN_CON Register 0 SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCK_TOP_CKHWEN_CON_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SCK_TOP_CKHWEN_CON_SET	**Sets up SCK_CKHWEN_CON** 1'b0: Not set 1'b1: Set

099C **SCK_TOP_CKHWEN_CON0_CLR** **SCK_CKHWEN_CON Register 0 CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCK_TOP_CKHWEN_CON_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SCK_TOP_CKHWEN_CON_CLR	**Clears SCK_CKHWEN_CON** 1'b0: Not clear 1'b1: Clear

09C6 **DCXO_CW00** **DCXO Code Word 0** **6B6D**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_CLKSEL_MAN	XO_ENBB_EN_M	XO_ENBB_MAN	XO_BB_LPM_EN	XO_EXTBUF4_EN_M	XO_EXTBUF4_MODE		XO_EXTBUF3_EN_M	XO_EXTBUF3_MODE		XO_EXTBUF2_EN_M	XO_EXTBUF2_MODE		XO_EXTBUF1_EN_M	XO_EXTBUF1_MODE	
Type	RW	RW	RW	RW	RW	RW		RW	RW		RW	RW		RW	RW	
Reset	0	1	1	0	1	0	1	1	0	1	1	0	1	1	0	1

Bit(s)	Name	Description
15	XO_CLKSEL_MAN	0: XO2~4 are controlled by pin (CLK_SEL). 1: XO2~4 are controlled by register XO_CLKSEL_MAN_EN. (Default)
14	XO_ENBB_EN_M	0: XO_SOC is disabled if manual (register) control. 1: XO_SOC is enabled if manual(register) control. (Default)
13	XO_ENBB_MAN	0: XO_SOC is controlled by pin (EN_BB).

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Bit(s)	Name	Description
		1: XO_SOC is controlled by register XO_ENBB_MAN_EN. (Default)
12	XO_BB_LPM_EN	**SW controlled LPM for saving power during transceiver standby** Must EN_BB=1, CLK_SEL=0.
11	XO_EXTBUF4_EN_M	**Enables/Disables XO_CEL during manual (register) control**
10:9	XO_EXTBUF4_MODE	00: Register controlled by XO_EXTBUF4_EN_M 01: EN_BB 10: CLK_SEL 11: XO_EXTBUF2_EN_M or XO_EXTBUF3_EN_M or CLK_SEL
8	XO_EXTBUF3_EN_M	**Enables/Disables XO_NFC during manual (register) control**
7:6	XO_EXTBUF3_MODE	00: Register controlled by XO_EXTBUF3_EN_M 01: EN_BB 10: CLK_SEL 11: XO_EXTBUF2_EN_M or XO_EXTBUF3_EN_M or CLK_SEL
5	XO_EXTBUF2_EN_M	**Enables/Disables XO_WCN during manual (register) control**
4:3	XO_EXTBUF2_MODE	00: Register controlled by XO_EXTBUF2_EN_M 01: EN_BB 10: CLK_SEL 11: XO_EXTBUF2_EN_M or XO_EXTBUF3_EN_M or CLK_SEL
2	XO_EXTBUF1_EN_M	**Enables/Disables XO_SOC during manual (register) control**
1:0	XO_EXTBUF1_MODE	00: Register controlled by XO_EXTBUF1_EN_M 01: EN_BB 10: CLK_SEL 11: EN_BB or CLK_SEL

09C8 **DCXO_CW00_SET** **DCXO Code Word 0 Set** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_CW00_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_CW00_SET	**Sets up DCXO Code Word 0** 0: Not set 1: Set

09CA **DCXO_CW00_CLR** **DCXO Code Word 0 Clear** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_CW00_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:0	DCXO_CW00_CLR	**Clears DCXO Code Word 0** 0: Not clear 1: Clear

09CC **DCXO_CW01** **DCXO Code Word 1** **6D55**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_BBLPM_CKSEL_M	XO_LPBUF_EN_M	XO_LPM_PREBUF_EN_M	XO_LPMBUF_MAN	XO_IBUF_EN_M	XO_PBUF_EN_M	XO_INTBUF_MAN	XO_EXTBUF4_CKG_EN_M	XO_EXTBUF4_CKG_MAN	XO_EXTBUF3_CKG_EN_M	XO_EXTBUF3_CKG_MAN	XO_EXTBUF2_CKG_EN_M	XO_EXTBUF2_CKG_MAN	XO_EXTBUF1_CKG_EN_M	XO_EXTBUF1_CKG_MAN	XO_CLKSEL_EN_M
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	0	1	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
15	XO_BBLPM_CKSEL_M	**XO_WCN and XO_CEL LPM frequency manually switched if XO_LPMBUF_MAN=1**
14	XO_LPBUF_EN_M	**XO low power buffer manually enable if XO_LPMBUF_MAN=1**
13	XO_LPM_PREBUF_EN_M	**XO low power buffer bias manually enable if XO_LPMBUF_MAN=1**
12	XO_LPMBUF_MAN	**XO low power buffer enable manual mode**
11	XO_IBUF_EN_M	**XO isolated buffer manually enable if XO_INTBUF_MAN=1**
10	XO_PBUF_EN_M	**XO pre-buffer manually enable if XO_INTBUF_MAN=1**
9	XO_INTBUF_MAN	**XO internal buffer enable manual mode**
8	XO_EXTBUF4_CKG_EN_M	**XO_CEL 26MHz output enable while manual mode**
7	XO_EXTBUF4_CKG_MAN	**XO_CEL 26MHz output enable manual mode**
6	XO_EXTBUF3_CKG_EN_M	**XO_NFC 26MHz output enable while manual mode**
5	XO_EXTBUF3_CKG_MAN	**XO_NFC 26MHz output enable manual mode**
4	XO_EXTBUF2_CKG_EN_M	**XO_WCN 26MHz output enable while manual mode**
3	XO_EXTBUF2_CKG_MAN	**XO_WCN 26MHz output enable manual mode**
2	XO_EXTBUF1_CKG_EN_M	**XO_SOC 26MHz output enable while manual mode**
1	XO_EXTBUF1_CKG_MAN	**XO_SOC 26MHz output enable manual mode**
0	XO_CLKSEL_EN_M	0: XO2~4 are disabled if manual (register) control. 1: XO2~4 are enabled if manual (register) control. (Default)

09CE **DCXO_CW02** **DCXO Code Word 2** **386A**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_BUFLDOK_EN	XO_26MLP_MAN_EN	XO_CBANK_SYNC_DYN	XO_LDOCAL_EN	XO_EN26M_OFFSQ_EN	XO_AAC_MODE_FPM		XO_AAC_MODE_LPM		XO_AAC_FPM_TIME		XO_STRUP_MODE	XO_XMODE_M	XO_XMODE_MAN	XO_EN32K_M	XO_EN32K_MAN
Type	RW	RW	RW	RW	RW	RW		RW		RW		RW	RW	RW	RW	RW
Reset	0	0	1	1	1	0	0	0	0	1	1	0	1	0	1	0

Bit(s)	Name	Description
15	XO_BUFLDOK_EN	**SW trigger external buffer LDO calibration**
14	XO_26MLP_MAN_EN	**Set high to always enable XO low power 26M to digital**
13	XO_CBANK_SYNC_DYN	0: The update clock of CBANK always turned on 1: The update clock of CBANK only turned on when CDAC is updated.
12	XO_LDOCAL_EN	0: Keep previous FPMLDO voltage setting 1: Trigger FPMLDO calibration (binary search) when entering FPM (default)
11	XO_EN26M_OFFSQ_EN	**Enables OFF sequence when 26M_EN=0**
10:9	XO_AAC_MODE_FPM	00: AAC 1st + 2nd steps (default) 01: Bypass and reuse previous value 10: AAC 1st only 11: Manual control bypass AAC
8:7	XO_AAC_MODE_LPM	00: AAC 1st + 2nd steps (default) 01: Bypass and reuse previous value 10: AAC 1st only 11: Manual control bypass AAC
6:5	XO_AAC_FPM_TIME	00: 16T32K 01: 32T32K 10: 64T32K 11: 128T32K (default)
4	XO_STRUP_MODE	0: Open OR close detection (default) 1: Open AND close detection
3	XO_XMODE_M	0: XMODE_G is disabled if manual (register) control. 1: XMODE_G is enabled if manual (register) control. (Default)
2	XO_XMODE_MAN	0: XMODE_G is controlled by pin (XMODE). (Default) 1: XMODE_G is controlled by register XO_XMODE_M.
1	XO_EN32K_M	0: EN_32K_G is disabled if manual (register) control. 1: EN_32K_G is enabled if manual (register) control. (Default)
0	XO_EN32K_MAN	0: EN_32K_G is controlled by pin (XO32K_EN). (Default) 1: EN_32K_G is controlled by register XO_EN32K_M.

09D0 **DCXO_CW03** **DCXO Code Word 3** **842B**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_FPM_ISEL_MAN					XO_LPM_ISEL_MAN					XO_EXTBUF7_CKG_EN_M	XO_EXTBUF7_CKG_MAN	XO_EXTBUF6_CKG_EN_M	XO_EXTBUF6_CKG_MAN	XO_PMU_CK_EN_MAN	XO_PMU_CK_EN_M
Type	RW					RW					RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	1	0	0	0	0	1	0	1	0	1	1

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Bit(s)	Name	Description
15:11	XO_FPM_ISEL_MAN	XO core FPM current settings if XO_AAC_MODE_LPM=11
10:6	XO_LPM_ISEL_MAN	XO core LPM current settings if XO_AAC_MODE_FPM=11
5	XO_EXTBUF7_CKG_EN_M	XO_EXT 26MHz output enable while manual mode
4	XO_EXTBUF7_CKG_MAN	XO_EXT 26MHz output enable manual mode
3	XO_EXTBUF6_CKG_EN_M	XO_PD 26MHz output enable while manual mode
2	XO_EXTBUF6_CKG_MAN	XO_PD 26MHz output enable manual mode
1	XO_PMU_CKEN_MAN	PMU 26M clock enable manual mode
0	XO_PMU_CKEN_M	PMU 26M clock manual control

09D2 **DCXO_CW04** **DCXO Code Word 4** **FF55**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_CDAC_LPM								XO_CDAC_FPM							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
15:8	XO_CDAC_LPM	XO CDAC code (complement) during LPM
7:0	XO_CDAC_FPM	XO CDAC code (complement) during FPM

09D4 **DCXO_CW05** **DCXO Code Word 5** **DD40**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_COFST_FPM		XO_32KDIV_NFRAC_FPM													
Type	RW		RW													
Reset	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	XO_COFST_FPM	XO CDAC offset code during FPM
13:0	XO_32KDIV_NFRAC_FPM	32K divider fractional input during FPM

09D6 **DCXO_CW06** **DCXO Code Word 6** **2318**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	XO_COFST_LPM		XO_32KDIV_NFRAC_LPM													
Type	RW		RW													
Reset	0	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0

Bit(s)	Name	Description
15:14	XO_COFST_LPM	XO CDAC offset code during LPM
13:0	XO_32KDIV_NFRAC_LPM	32K divider fractional input during LPM

09D8 **DCXO_CW07** **DCXO Code Word 7** **8FFE**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_CORE_IDAC_FPM		XO_CORE_GMX2_FPM	XO_CORE_BYPCAS_FPM	XO_ILPM_COMP_EN_M	XO_IFPM_COMP_EN_M	XO_IAAC_COMP_EN_M	XO_VTCGEN_EN_M	XO_LPMBIAS_EN_M	XO_CORE_VBLPM_EN_M	XO_CORE_VBFPM_EN_M	XO_STARTUP_EN_M	XO_CORE_AAC_EN_M	XO_CORE_TURBO_EN_M	XO_CORE_EN_M	XO_CORE_MAN
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0

Bit(s)	Name	Description
15:14	XO_CORE_IDAC_FPM	XO gm core current control during FPM or XO_CORE_MAN=1
13	XO_CORE_GMX2_FPM	XO core Gm double option during FPM or XO_CORE_MAN=1
12	XO_CORE_BYPCAS_FPM	XO core bypass cascode option during FPM or XO_CORE_MAN=1
11	XO_ILPM_COMP_EN_M	Enables XO ILPM to comparator if XO_CORE_MAN=1
10	XO_IFPM_COMP_EN_M	Enables XO IFPM to comparator if XO_CORE_MAN=1
9	XO_IAAC_COMP_EN_M	Enables XO IAAC to comparator if XO_CORE_MAN=1
8	XO_VTCGEN_EN_M	Enables FPM gm bias circuit if XO_CORE_MAN=1
7	XO_LPMBIAS_EN_M	Enables XO core LPM bias circuit if XO_CORE_MAN=1
6	XO_CORE_VBLPM_EN_M	Enables XO core LPM bias if XO_CORE_MAN=1
5	XO_CORE_VBFPM_EN_M	Enables XO core FPM bias if XO_CORE_MAN=1
4	XO_STARTUP_EN_M	XO core startup gating option if XO_CORE_MAN=1
3	XO_CORE_AAC_EN_M	Enables XO core AAC bias if XO_CORE_MAN=1
2	XO_CORE_TURBO_EN_M	XO core iturbo option if XO_CORE_MAN=1
1	XO_CORE_EN_M	Enables XO oscillator core if XO_CORE_MAN=1
0	XO_CORE_MAN	XO core manual mode

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09DA **DCXO_CW08** **DCXO Code Word 8** **46BE**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_AAC_COMP_POL	XO_AAC_VSEL_FPM				XO_AAC_COMP_HV_FPM	XO_AAC_VOFST_FPM		XO_AAC_IBIAS_FPM		XO_AAC_HV_FPM	XO_COMP_TSTEN_M	XO_COMP_EN_M	XO_AAC_MONEN_M	XO_AAC_EN_M	XO_AAC_COMP_MAN
Type	RW	RW				RW	RW		RW		RW	RW	RW	RW	RW	RW
Reset	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	0

Bit(s)	Name	Description
15	XO_AAC_COMP_POL	Inverse the polarity of AD_XO_AAC_COMP_OUT for mistake in case
14:11	XO_AAC_VSEL_FPM	XO AAC target peak-to-peak amplitude during FPM or XO_AAC_COMP_MAN=1
10	XO_AAC_COMP_HV_FPM	XO AAC COMP high amplitude mode during FPM or XO_AAC_COMP_MAN=1
9:8	XO_AAC_VOFST_FPM	XO AAC input offset settings during FPM or XO_AAC_COMP_MAN=1
7:6	XO_AAC_IBIAS_FPM	XO AAC bias current settings during FPM or XO_AAC_COMP_MAN=1
5	XO_AAC_HV_FPM	XO AAC high amplitude mode during FPM or XO_AAC_COMP_MAN=1
4	XO_COMP_TSTEN_M	XO COMP voltage testing mode during startup or XO_AAC_COMP_MAN=1
3	XO_COMP_EN_M	Enables XO COMP during AAC or XO_AAC_COMP_MAN=1
2	XO_AAC_MONEN_M	XO AAC voltage monitor mode during startup or XO_AAC_COMP_MAN=1
1	XO_AAC_EN_M	XO AAC enable during AAC or XO_AAC_COMP_MAN=1
0	XO_AAC_COMP_MAN	XO AAC/COMP manual mode

09DC **DCXO_CW09** **DCXO Code Word 9** **010F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_SWRST	XO_AAC_FPM_SWEN	XO_AAC_VOFST_LPM		XO_AAC_IBIAS_LPM		XO_AAC_HV_LPM	XO_AAC_VSEL_LPM				XO_AAC_COMP_HV_LPM	XO_CORE_IDAC_LPM		XO_CORE_GMX2_LPM	XO_CORE_BYPCAS_LPM
Type	RW	RW	RW		RW		RW	RW				RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
15	XO_SWRST	**XO digital macro software reset**
14	XO_AAC_FPM_SWEN	0: Disable 1: SW trigger AAC during FPM
13:12	XO_AAC_VOFST_LPM	**XO AAC input offset settings during LPM**

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Bit(s)	Name	Description
11:10	XO_AAC_IBIAS_LPM	**XO AAC bias current settings during LPM**
9	XO_AAC_HV_LPM	**XO AAC high amplitude mode during LPM**
8:5	XO_AAC_VSEL_LPM	**XO AAC target peak-to-peak amplitude during LPM**
4	XO_AAC_COMP_HV_LPM	**XO AAC COMP high amplitude mode during LPM**
3:2	XO_CORE_IDAC_LPM	**XO gm core current control during LPM**
1	XO_CORE_GMX2_LPM	**XO core Gm double option during LPM**
0	XO_CORE_BYPCAS_LPM	**XO core bypass cascode option during LPM**

09DE **DCXO_CW10** **DCXO Code Word 10** **EF50**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**XO_VBIST_EN_M**	**XO_TEST_VCAL_EN_M**	**XO_LDOVTST_EN_M**	**XO_LDOPBUF_VSET_M**				**XO_LDOPBUF_EN_M**	**XO_LDO_MAN**	**XO_CTL_SYNC_EN_M**	**XO_CTL_SYNC_MAN**	**XO_CBANK_SYNC_EN_M**	**XO_CBANK_SYNC_MAN**	**XO_32KDIV_TEST_EN**	**XO_32KDIV_RATIO_MAN**	**XO_32KDIV_SWRST**
Type	RW	RW	RW	RW				RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	0	1	1	1	1	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
15	XO_VBIST_EN_M	Enables XO self voltage calibration monitor path if XO_LDO_MAN=1
14	XO_TEST_VCAL_EN_M	Enables XO self voltage calibrated mode if XO_LDO_MAN=1
13	XO_LDOVTST_EN_M	Enables XO PBUF LDO voltage testmux if XO_LDO_MAN=1
12:9	XO_LDOPBUF_VSET_M	XO PBUF LDO output voltage manual settings if XO_LDO_MAN=1
8	XO_LDOPBUF_EN_M	Enables XO internal buffer bias if XO_LDO_MAN=1
7	XO_LDO_MAN	XO LDO enable manual mode
6	XO_CTL_SYNC_EN_M	Enables CTL SYNC if XO_SYNC_MAN=1
5	XO_CTL_SYNC_MAN	XO local CTL sync enable manual mode
4	XO_CBANK_SYNC_EN_M	Enables CBANK SYNC if XO_CBANK_SYNC_MAN=1
3	XO_CBANK_SYNC_MAN	XO local CBANK sync enable manual mode
2	XO_32KDIV_TEST_EN	DCXO 32K divider testing output thru DCXO_AUXOUT
1	XO_32KDIV_RATIO_MAN	Manually control set the ratio of 32K divider high
0	XO_32KDIV_SWRS	32K digital divider software reset

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Bit(s)	Name	Description
	T	

09E0 DCXO_CW11 DCXO Code Word 11 AD00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_BUF1LDO_CAL_M	XO_BUFLDOK_MAN	XO_EXTBUF7_EN_M	XO_EXTBUF7_MODE		XO_EXTBUF6_EN_M	XO_EXTBUF6_MODE		XO_RESERVED3			XO_VTEST_SEL_MUX				
Type	RW	RW	RW	RW		RW	RW		RW			RW				
Reset	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	XO_BUF1LDO_CAL_M	**Enables/Disables BUF1LDO CAL during manual (register) control**
14	XO_BUFLDOK_MAN	**EXTBUF LDO CAL enable manual mode**
13	XO_EXTBUF7_EN_M	**Enables/Disables XO_EXT during manual (register) control**
12:11	XO_EXTBUF7_MODE	00: Register controlled by XO_EXTBUF7_EN_M 01: EN_BB 10: CLK_SEL 11: EN_BB or CLK_SEL
10	XO_EXTBUF6_EN_M	**Enables/Disables XO_PD during manual (register) control**
9:8	XO_EXTBUF6_MODE	00: Register controlled by XO_EXTBUF6_EN_M 01: EN_BB 10: CLK_SEL 11: EN_BB or CLK_SEL
7:5	XO_RESERVED3	**Register reserved**
4:0	XO_VTEST_SEL_MUX	**XO testmux selection MUX**

09E2 DCXO_CW11_SET DCXO Code Word 11 Set 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_CW11_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_CW11_SET	**DCXO Code Word 11 Set** 0: No Set 1: Set

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09E4 **DCXO_CW11_CLR** **DCXO Code Word 11 Clear** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_CW11_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_CW11_CLR	**DCXO Code Word 11 Clear** 0: No Clear 1: Clear

09E6 **DCXO_CW12** **DCXO Code Word 12** **8A75**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_XO_LDOPBUF_ENCL	RG_XO_LDOPBUF_BYP	RG_XO_LPBUF_INV	RG_XO_CTL_SYNC_BYP	RG_XO_CTL_POL	RG_XO_CBANK_SYNC_BYP	RG_XO_CBANK_POL	RG_XO_SYNC_CKPOL	XO_THADC_EN	RG_XO_CORE_OSCTD		XO_CAL_EN_M	XO_CAL_EN_MAN	XO_VIO18PG_BUFEN	XO_EXTBUF4_CLKSEL_MAN	XO_BUFLDO_CAL_M
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW
Reset	1	0	0	0	1	0	1	0	0	1	1	1	0	1	0	1

Bit(s)	Name	Description
15	RG_XO_LDOPBUF_ENCL	**Enable signal for XO PBUFLDO closed loop**
14	RG_XO_LDOPBUF_BYP	**Enable signal for XO PBUFLDO bypass mode**
13	RG_XO_LPBUF_INV	**XO control signal of clock inversion for low power buffer chain**
12	RG_XO_CTL_SYNC_BYP	**XO control signal for bypassing bias control local synchronization**
11	RG_XO_CTL_POL	**XO control signal of clock polarity for bias control local synchronization** 0: Positive edge, 1: falling edge
10	RG_XO_CBANK_SYNC_BYP	**XO control signal for bypassing CBank control local synchronization**
9	RG_XO_CBANK_POL	**XO control signal of clock polarity for CBank control local synchronization** 0: Positive edge, 1: falling edge
8	RG_XO_SYNC_CKPOL	**XO control signal of local synchronized clock polarity** 0: In-phase of X1 1: Out-of-phase of X1
7	XO_THADC_EN	**Enables Vbe monitor by AUXADC** For XO temperature sensing.
6:5	RG_XO_CORE_OSCTD	**DCXO control signal for startup delay controls (open-loop)**
4	XO_CAL_EN_M	**Enables CAL_EN manual when XO_CAL_EN_MAN=1**
3	XO_CAL_EN_MAN	**CAL_EN manual control mux**
2	XO_VIO18PG_BUF	**Buffer enable is gated by VIO18_PG or not**

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Bit(s)	Name	Description
	EN	
1	XO_EXTBUF4_CLKSEL_MAN	0: Enable/Disable XO_CEL from pin control 1: Enable/Disable XO_CEL from register
0	XO_BUFLDO_CAL_M	**Enables/Disables BUFLDO CAL during manual (register) control**

09E8 DCXO_CW13 DCXO Code Word 13 9829

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_XO_RESERVED5			RG_XO_BUFLDO24_IBX2	RG_XO_BUFLDO24_ENCL	RG_XO_VOW_DIV		RG_XO_VOW_EN	RG_XO_RESERVED4		RG_XO_IBUF_ISET		RG_XO_PBUF_ISET		RG_XO_VGBIAS_VSET	
Type	RW			RW	RW	RW		RW	RW		RW		RW		RW	
Reset	1	0	0	1	1	0	0	0	0	0	1	0	1	0	0	1

Bit(s)	Name	Description
15:13	RG_XO_RESERVED5	**Register reserved**
12	RG_XO_BUFLDO24_IBX2	**XO control signal of bias current doubler on EXTBUF24 LDO**
11	RG_XO_BUFLDO24_ENCL	**Enable signal of EXTBUF24 LDO closed loop**
10:9	RG_XO_VOW_DIV	00: 26M 01: 26M/2 10: 26M/4 11: 26M/8
8	RG_XO_VOW_EN	**26MHz clk for VOW use**
7:6	RG_XO_RESERVED4	**Register reserved**
5:4	RG_XO_IBUF_ISET	**XO control signal of internal isolated buffer current**
3:2	RG_XO_PBUF_ISET	**XO control signal of FPM pre-buffer current**
1:0	RG_XO_VGBIAS_VSET	**XO input gate bias control during FPM**

09EA DCXO_CW14 DCXO Code Word 14 A2B5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_XO_AUDIO_ATTEN		XO_AUDIO_EN_M	XO_EXTBUF2_CLKSEL_MAN	RG_XO_RESERVED0	RG_XO_EXTBUF_INV	RG_XO_LVLDO_RFB		RG_XO_BUFLDO67_IX2	RG_XO_BUFLDO67_IBX2	RG_XO_BUFLDO67_ENCL	RG_XO_LVLDO_I_CTRL		RG_XO_BUFLDO13_IX2	RG_XO_BUFLDO13_IBX2	RG_XO_BUFLDO13_ENCL
Type	RW		RW	RW	RW	RW	RW		RW	RW	RW	RW		RW	RW	RW
Reset	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1

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Bit(s)	Name	Description
15:14	RG_XO_AUDIO_ATTEN	XO control signal of RC filter on LP path
13	XO_AUDIO_EN_M	XO_AUDIO_EN_M
12	XO_EXTBUF2_CLKSEL_MAN	XO_EXTBUF2_CLKSEL_MAN
11	RG_XO_RESERVED0	Reserved register 0
10	RG_XO_EXTBUF_INV	XO control signal of clock inversion for low noise external buffer
9:8	RG_XO_LVLDO_RFB	Selects LVLDO Vout
7	RG_XO_BUFLDO67_IX2	XO control signal of double current on EXTBUF67 LDO
6	RG_XO_BUFLDO67_IBX2	XO control signal of bias current doubler on EXTBUF67 LDO
5	RG_XO_BUFLDO67_ENCL	Enable signal of EXTBUF67 LDO closed loop
4:3	RG_XO_LVLDO_I_CTRL	Selects LVLDO current
2	RG_XO_BUFLDO13_IX2	XO control signal of double current on EXTBUF13 LDO
1	RG_XO_BUFLDO13_IBX2	XO control signal of bias current doubler on EXTBUF13 LDO
0	RG_XO_BUFLDO13_ENCL	Enable signal of EXTBUF13 LDO closed loop

09EC **DCXO_CW15** **DCXO Code Word 15** **A19A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_XO_EXTBUF7_HD		RG_XO_EXTBUF6_HD		RG_XO_RESERVED8		RG_XO_EXTBUF4_HD		RG_XO_EXTBUF3_HD		RG_XO_EXTBUF2_HD		RG_XO_EXTBUF1_HD		RG_XO_AUDIO_ISET	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	0	1	0	0	0	0	1	1	0	0	1	1	0	1	0

Bit(s)	Name	Description
15:14	RG_XO_EXTBUF7_HD	XO control signal of EXTBUF7 output driving strength
13:12	RG_XO_EXTBUF6_HD	XO control signal of EXTBUF6 output driving strength
11:10	RG_XO_RESERVED8	Register reserved
9:8	RG_XO_EXTBUF4_HD	XO control signal of EXTBUF4 output driving strength
7:6	RG_XO_EXTBUF3_HD	XO control signal of EXTBUF3 output driving strength
5:4	RG_XO_EXTBUF2_HD	XO control signal of EXTBUF2 output driving strength
3:2	RG_XO_EXTBUF1_HD	XO control signal of EXTBUF1 output driving strength
1:0	RG_XO_AUDIO_IS	XO control signal of LP buffer current

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Bit(s)	Name	Description
	ET	

09EE DCXO_CW16 DCXO Code Word 16 A8AA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_XO_LPM_PREBUF_ISET		XO_EXTBUF7_ISET_M		XO_EXTBUF6_ISET_M		XO_RESERVED9		XO_EXTBUF4_ISET_M		XO_EXTBUF3_ISET_M		XO_EXTBUF2_ISET_M		XO_EXTBUF1_ISET_M	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
15:14	RG_XO_LPM_PREBUF_ISET	Current settings for 26MHz low power pre-buffer
13:12	XO_EXTBUF7_ISET_M	XO control signal of current on EXTBUF7
11:10	XO_EXTBUF6_ISET_M	XO control signal of current on EXTBUF6
9:8	XO_RESERVED9	Register reserved
7:6	XO_EXTBUF4_ISET_M	XO control signal of current on EXTBUF4
5:4	XO_EXTBUF3_ISET_M	XO control signal of current on EXTBUF3
3:2	XO_EXTBUF2_ISET_M	XO control signal of current on EXTBUF2
1:0	XO_EXTBUF1_ISET_M	XO control signal of current on EXTBUF1

09F0 DCXO_CW17 DCXO Code Word 17 7773

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_BUFLDO67_VSET_M				XO_BUFLDO24_VSET_M				XO_BUFLDO13_VSET_M				RG_XO_TSOURCE_EN	XO_THADC_EN_MAN	RG_XO_RESERVED1	
Type	RW				RW				RW				RW	RW	RW	
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	0	1	1

Bit(s)	Name	Description
15:12	XO_BUFLDO67_VSET_M	XO control signal of EXTBUF67 LDO voltage
11:8	XO_BUFLDO24_VSET_M	XO control signal of EXTBUF24 LDO voltage
7:4	XO_BUFLDO13_VSET_M	XO control signal of EXTBUF13 LDO voltage
3	RG_XO_TSOURCE_EN	Enables thermal source for thermal calibration
2	XO_THADC_EN_MAN	THADC enable manual mode

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Bit(s)	Name	Description
1:0	RG_XO_RESERVED1	Reserved register 1

09F2 **DCXO_CW18** **DCXO Code Word 18** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_AUXOUT_SEL										XO_STATIC_AUXOUT_SEL					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:6	XO_AUXOUT_SEL	Selects dynamic AuxOut
5:0	XO_STATIC_AUXOUT_SEL	Selects static AuxOut

09F4 **DCXO_CW19** **DCXO Code Word 19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_STATIC_AUXOUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XO_STATIC_AUXOUT	Static Auxout Readout

09F6 **DCXO_CW20** **DCXO Code Word 20** **0011**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_XO_RESRVED10											RG_XO_CORNER_DETECT_EN_MAN	RG_XO_CORNER_DETECT_EN	RG_XO_HEATER_SEL		RG_XO_PCTAT_COMP_EN
Type	RW											RW	RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

Bit(s)	Name	Description
15:5	RG_XO_RESRVED10	
4	RG_XO_CORNER_DETECT_EN_MAN	
3	RG_XO_CORNER_DETECT_EN	

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Bit(s)	Name	Description
2:1	RG_XO_HEATER_SEL	
0	RG_XO_PCTAT_COMP_EN	Control for cap bias corner calibration and heater

09F8 DCXO_CW21 DCXO Code Word 21 02A7

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_XO_RESRVED11						RG_XO_CORNER_SETTING_TUNE									
Type	RW						RW									
Reset	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	1

Bit(s)	Name	Description
15:10	RG_XO_RESRVED11	
9:0	RG_XO_CORNER_SETTING_TUNE	

09FA DCXO_CW22 DCXO Code Word 22 0280

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							XO_PTATCTAT_EN_FPM	XO_PTATCTAT_EN_LPM	XO_PTATCTAT_EN_M	XO_PTATCTAT_EN_MAN	XO_MDB_TBO_EN_SEL	RGS_AD_XO_CORNER_SEL				RGS_AD_XO_CORNER_CAL_DONE
Type							RW	RW	RW	RW	RW	RO				RO
Reset							1	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	XO_PTATCTAT_EN_FPM	
8	XO_PTATCTAT_EN_LPM	
7	XO_PTATCTAT_EN_M	
6	XO_PTATCTAT_EN_MAN	
5	XO_MDB_TBO_EN_SEL	**Selects MDB tri-state buffer output enable control** 0: From DIR TOP 1: From DCXO local control
4:1	RGS_AD_XO_CORNER_SEL	
0	RGS_AD_XO_CORNER_CAL_DONE	

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09FE DCXO_ELR0 DCXO ELR 0 Register 0008

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_XO_GS_VTEMP			RG_XO_PCTAT_RDEG_SEL
Type													RW			RW
Reset													1	0	0	0

Bit(s)	Name	Description
3:1	RG_XO_GS_VTEMP	Calibrates RG_XO_GS_VTEMP
0	RG_XO_PCTAT_RDEG_SEL	Calibrates RG_XO_PCTAT_RDEG_SEL

0A08 RTC_BBPU Baseband Power Up 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY_BBPU									CBUSY	RELOAD	CLRPKY	AUTO	BBPU		PWREN
Type	WO									RO	WO	WO	RW	RW		RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0		0

Bit(s)	Name	Description
15:8	KEY_BBPU	**A bus write is acceptable only when KEY_BBPU=0x43.**
6	CBUSY	**The read/write channels between RTC/Core is busy.** This bit indicates high after software program sequence to anyone of RTC data registers and enable the transfer by RTC_WRTGR=1. It is high after the reset from low to high because RTC reload process.
5	RELOAD	**Reloads the values from RTC domain to Core domain** RTC will reload to synchronize the data from RTC to core when reset from 0 to 1. This bit can be treated as the debug bit.
4	CLRPKY	**Clears powerkey1 and powerkey2 at the same time** In some cases, software may clear powerkey1 and powerkey2. BBWAKEUP depends on the matching specific patterns of powerkey1 and powerkey2. If any one of powerkey1 or powerkey2 or BBPU is cleared, BBWAKEUP will go low immediately. Software cannot program other control bits without power. By programming RTC_BBPU with CLRPKY=1 and BBPU=0, RTC can clear powerkey1, powerkey2 and BBPU at the same moment.
3	AUTO	**Clears SPAR Event in old legacy mode when SYSRST# transits from high to low** 0: BBWAKEUP is not automatically in the low state when SYSRST# transits from high to low. 1: BBWAKEUP is automatically in the low state when SYSRST# transits from high to low. The function is only active when RTC_POWERKEY1 and RTC_POWERKEY2 match the correct values.
2	BBPU	**Wake-up event of PMIC** If powerkey1=A357h and powerkey2=67D2h, PMIC will take the value programmed by software; otherwise PMIC will be low. 0: SW clears SPAR/Alarm.

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Bit(s)	Name	Description
		1: For debugging
0	PWREN	0: RTC alarm has no action on power switch. 1: When an RTC alarm occurs, alarm start-up is set to 1 and the system is powered on by RTC alarm wakeup.

0A0A **RTC_IRQ_STA** **RTC IRQ Status** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													LPSTA		TCSTA	ALSTA
Type													RO		RO	RO
Reset													0		0	0

Bit(s)	Name	Description
3	LPSTA	**Indicates the IRQ status and whether or not the LPD is asserted** 0: No IRQ occurs. The 32K clock is good. 1: IRQ occurs The 32K clock stopped or stops. This can be masked by LP_EN or cleared by initializing LPD.
1	TCSTA	**This register indicates the IRQ status and whether or not the tick condition has been met.** 0: No IRQ occurs. The tick condition has not been met. 1: IRQ occurred; the tick condition has been met.
0	ALSTA	**This register indicates the IRQ status and whether or not the alarm condition has been met.** 0: No IRQ occurred; the alarm condition has not been met. 1: IRQ occurred; the alarm condition has been met.

0A0C **RTC_IRQ_EN** **RTC IRQ Enable** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													LP_EN	ONESHOT	TC_EN	AL_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	LP_EN	**This register enables the control bit for IRQ generation if the Low power detected (32k clock off).** 0: Disable IRQ generations. 1: Enable the LPD.
2	ONESHOT	**Controls automatic reset of AL_EN and TC_EN.**
1	TC_EN	**Enables the control bit for IRQ generation if the tick condition has been met** 0: Disable IRQ generations. 1: Enable tick time match interrupt. Clear the interrupt when ONESHOT is high upon generation of the corresponding IRQ.
0	AL_EN	**Enables the control bit for IRQ generation if the alarm condition has been met**

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Bit(s)	Name	Description
		0: Disable IRQ generations 1: Enable alarm time match interrupt. Clear the interrupt when ONESHOT is high upon generation of the corresponding IRQ.

0A0E RTC_CII_EN Counter Increment IRQ Enable 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SECCII_1_8	SECCII_1_4	SECCII_1_2	YEACII	MTHCII	DOWCII	DOMCII	HOUCII	MINCII	SECCII
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	SECCII_1_8	Set the bit to 1 to activate the IRQ at each one-eighth of a second update.
8	SECCII_1_4	Set the bit to 1 to activate the IRQ at each one-fourth of a second update.
7	SECCII_1_2	Set the bit to 1 to activate the IRQ at each one-half of a second update.
6	YEACII	Set the bit to 1 to activate the IRQ at each year update.
5	MTHCII	Set the bit to 1 to activate the IRQ at each month update.
4	DOWCII	Set the bit to 1 to activate the IRQ at each day-of-week update.
3	DOMCII	Set the bit to 1 to activate the IRQ at each day-of-month update.
2	HOUCII	Set the bit to 1 to activate the IRQ at each hour update.
1	MINCII	Set the bit to 1 to activate the IRQ at each minute update.
0	SECCII	Set this bit to 1 to activate the IRQ at each second update.

0A10 RTC_AL_MASK RTC Alarm Mask 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										YEA_MSK	MTH_MSK	DOW_MSK	DOM_MSK	HOU_MSK	MIN_MSK	SEC_MSK
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	YEA_MSK	0: Condition (RTC_TC_YEA = RTC_AL_YEA) is checked to generate the alarm signal. 1: Condition (RTC_TC_YEA = RTC_AL_YEA) is masked, i.e. the value of RTC_TC_YEA does not affect the alarm IRQ generation.
5	MTH_MSK	0: Condition (RTC_TC_MTH = RTC_AL_MTH) is checked to generate the alarm signal. 1: Condition (RTC_TC_MTH = RTC_AL_MTH) is masked, i.e. the value of RTC_TC_MTH does not affect the alarm IRQ generation.
4	DOW_MSK	0: Condition (RTC_TC_DOW = RTC_AL_DOW) is checked to generate the alarm signal. 1: Condition (RTC_TC_DOW = RTC_AL_DOW) is masked, i.e. the value of RTC_TC_DOW does not affect the alarm IRQ generation.
3	DOM_MSK	0: Condition (RTC_TC_DOM = RTC_AL_DOM) is checked to generate the alarm signal.

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Bit(s)	Name	Description
		1: Condition (RTC_TC_DOM = RTC_AL_DOM) is masked, i.e. the value of RTC_TC_DOM does not affect the alarm IRQ generation.
2	HOU_MSK	0: Condition (RTC_TC_HOU = RTC_AL_HOU) is checked to generate the alarm signal. 1: Condition (RTC_TC_HOU = RTC_AL_HOU) is masked, i.e. the value of RTC_TC_HOU does not affect the alarm IRQ generation.
1	MIN_MSK	0: Condition (RTC_TC_MIN = RTC_AL_MIN) is checked to generate the alarm signal. 1: Condition (RTC_TC_MIN = RTC_AL_MIN) is masked, i.e. the value of RTC_TC_MIN does not affect the alarm IRQ generation.
0	SEC_MSK	0: Condition (RTC_TC_SEC = RTC_AL_SEC) is checked to generate the alarm signal. 1: Condition (RTC_TC_SEC = RTC_AL_SEC) is masked, i.e. the value of RTC_TC_SEC does not affect the alarm IRQ generation.

0A12 **RTC_TC_SEC** **RTC Seconds Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TC_SECOND					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	TC_SECOND	**Second initial value for the time counter** Range: 0~59

0A14 **RTC_TC_MIN** **RTC Minutes Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TC_MINUTE					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	TC_MINUTE	**Minute initial value for the time counter** Range: 0~59

0A16 **RTC_TC_HOU** **RTC Hours Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TC_HOUR				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TC_HOUR	Hour initial value for the time counter

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Bit(s)	Name	Description
		Range: 0~23

0A18 RTC_TC_DOM RTC Day-of-month Time Counter Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TC_DOM				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TC_DOM	**Day-of-month initial value for the time counter** The day-of-month maximum value depends on the leap year condition, i.e. 2 LSB of year time counter are 0.

0A1A RTC_TC_DOW RTC Day-of-Week time Counter Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														TC_DOW		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	TC_DOW	**Day-of-week initial value for the time counter** Range: 1~7

0A1C RTC_TC_MTH RTC Month Time Counter Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TC_MONTH			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TC_MONTH	**Month initial value for the time counter** Range: 1~12

0A1E RTC_TC_YEA RTC Year Time Counter Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TC_YEAR						
Type										RW						
Reset										0	0	0	0	0	0	0

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Bit(s)	Name	Description
6:0	TC_YEAR	**Year initial value for the time counter** Range: 0~127 (2000~2127) Software can bias the year as multiples of 4 for the internal leap-year formula, e.g. 2000~2127, 1972~2099, 1904~2031. To simplify it, RTC hardware treats all 4-multiple as leap years. If the range you defined includes non-leap 4-multiple year (e.g. 2100), adjust it to the correct date (e.g. change Feb. 29th, 2100 to Mar. 1st, 2100). It is suggested to bias the range larger than 1900 and less than 2100 to evade the manual adjustment, i.e. the bias values are suggested to be in the range of [-28,-96], which means (1972~2099) ~ (1904~2031). Formal leap formula: if year modulo 400 is 0 then leap else if year modulo 100 is 0 then no_leap else if year modulo 4 is 0 then leap else no_leap

0A20 **RTC_AL_SEC** **RTC Second Alarm Setting Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	K_EOSC32_VTCXO_ON_SEL	RTC_LPD_OPT		BBPU_2SEC_STAT_STA	BBPU_2SEC_STAT_CLEAR	BBPU_2SEC_MODE		BBPU_2SEC_EN	BBPU_2SEC_CK_SEL	BBPU_AUTO_PDN_SEL	AL_SECOND					
Type	RW	RW		RO	WO	RW		RW	RW	RW	RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	K_EOSC32_VTCXO_ON_SEL	**The bit is only valid when EMBCK_SEL_MODE is set to EMB_K_EOSC32 mode** 0: VTCXO controlled by HW 1: VTCXO always on
14:13	RTC_LPD_OPT	**f32k_ck_alive setting (rstb of LPSTA_RAW)** Depends on XOSC LPDETB (xosc32_ck_alive) or EOSC LPDETB (eosc32_ck_alive) 2'b11: Always 1 2'b10: xosc32_ck_alive (triggered when clock stops) 2'b01: eosc32_ck_alive (triggered when VRTC low-V) 2'b00: xosc32_ck_alive & eosc32_ck_alive
12	BBPU_2SEC_STAT_STA	**Bbwakeup 2 sec status** 1'b0: 2 sec reboot did not happened before. 1'b1: 2 sec reboot happened before.
11	BBPU_2SEC_STAT_CLEAR	**Clears Bbwakeup 2 sec event** Read back as BBPU_2SEC_STAT.
10:9	BBPU_2SEC_MODE	2'b11: Never power down 2'b10: 2 sec power down after battery is removed 2'b01: 1 sec power down after battery is removed 2'b00: 0.5 sec power down after battery is removed
8	BBPU_2SEC_EN	0: Legacy mode 1: 2 sec power down mode
7	BBPU_2SEC_CK_SEL	0: embck_ck 1: eosc32_ck

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Bit(s)	Name	Description
6	BBPU_AUTO_PDN_SEL	0: Original 2 sec reboot feature 1: Support both 2 sec reboot and auto_pdn
5:0	AL_SECOND	**Second value of the alarm counter setting** Range: 0~59

0A22 **RTC_AL_MIN** **RTC Minute Alarm Setting Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AL_MINUTE					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	AL_MINUTE	**Minute value of the alarm counter setting** Range: 0~59

0A24 **RTC_AL_HOU** **RTC Hour Alarm Setting Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NEW_SPARE0											AL_HOUR				
Type	RW											RW				
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
15:8	NEW_SPARE0	**NEW_SPARE0[7]:** WO: Reset bat status by writing 1, auto clear 0 NEW_SPARE0[6]: RO: 0 = no bat now/1 = bat installed properly NEW_SPARE0[5]: RO: 0 = battery always exists/1 = battery has been removed NEW_SPARE0[4:0]: Battery removed time counter (unit: minute) stopped when counting to 5'd30; reset to 0 by SPARE0[7]
4:0	AL_HOUR	**Hour value of the alarm counter setting** Range: 0~23

0A26 **RTC_AL_DOM** **RTC Day-of-month Alarm Setting Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NEW_SPARE1											AL_DOM				
Type	RW											RW				
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
15:8	NEW_SPARE1	**Rsv REGs for debugging**

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Bit(s)	Name	Description
4:0	AL_DOM	**Day-of-month value of the alarm counter setting** The day-of-month maximum value depends on the leap year condition, i.e. 2 LSB of year time counter are 0.

0A28 **RTC_AL_DOW** **RTC Day-of-week Alarm Setting Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NEW_SPARE2													AL_DOW		
Type	RW													RW		
Reset	0	0	0	0	0	0	0	0						0	0	0

Bit(s)	Name	Description
15:8	NEW_SPARE2	**Reserved for specific purposes**
2:0	AL_DOW	**Day-of-week value of the alarm counter setting** Range: 1~7

0A2A **RTC_AL_MTH** **RTC Month Alarm Setting Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NEW_SPARE3												AL_MONTH			
Type	RW												RW			
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15:8	NEW_SPARE3	**Reserved for specific purposes**
3:0	AL_MONTH	**Month value of the alarm counter setting** Range: 1~12

0A2C **RTC_AL_YEA** **RTC Year Alarm Setting Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										AL_YEAR						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	AL_YEAR	**Year value of the alarm counter setting** Range: 0~127 (2000~2127)

0A2E **RTC_OSC32CON** **OSC32 Control** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name		RTC_GP_OSC32_CON		RTC_EOSC32_CHOP_EN	RTC_EOSC32_VCT_EN	RTC_EOSC32_OPT	RTC_EMBCK_SEL_OPTION	RTC_EMBCK_SRC_SEL	RTC_EMBCK_SEL_MODE			XOSCCALI				
Type		RW		RW	RW	RW	RW	RW	RW			RW				
Reset		0	0	0	0	0	0	0	0	0		0	0	0	0	0

Bit(s)	Name	Description
14:13	RTC_GP_OSC32_CON	**EOSC32 RSV**
12	RTC_EOSC32_CHOP_EN	**Enables EOSC32 chopper** When chopper is disabled, the current consumption can become lower; however, eosc32_ck might become unstable. When powerkeys do not match, the chopper will be enabled. 0: Disable 1: Enable
11	RTC_EOSC32_VCT_EN	**Enables EOSC32 threshold tracking** 0: Disable 1: Enable
10	RTC_EOSC32_OPT	
9	RTC_EMBCK_SEL_OPTION	**Embedded clock selection option after battery removal** Note: Set this bit to 1'b1 to extend the embedded clock life time after battery removal with a poorer clock source. EOSC32 can only keep the spec before LPD. After LPD, the frequency drift will become larger. 0: Embedded clock switching back to dcxo decided by (eosc32_ck_alive & powerkey_match) 1: Embedded clock switching back to dcxo decided by (powerkey_match)
8	RTC_EMBCK_SRC_SEL	**Selects embedded clock source selection in EMB_K_EOSC32 mode (RTC_OSC32CON[7:6]=2'b01)** 0: f32k_ck src = dcxo_ck 1: f32k_ck src = eosc32_ck
7:6	RTC_EMBCK_SEL_MODE	**Embedded clock source selection mode:** 00:EMB_SW_DCXO mode (from bit6). f32k_ck src = dcxo_ck 01:EMB_SW_EOSC32 mode(from bit6). f32k_ck src = eosc32_ck 10:EMB_K_EOSC32 mode. Initial f32k_ck source = DCXO; SW can configure f32k_ck src by configuring RTC_OSC32CON[8] (EMBCK_SEL). HW automatically switches f32k_ck src to eosc32_ck at VBAT LV level. 11:EMB_HW (embedded HW) mode. Initial f32k_ck source = DCXO; hardware automatically switches to EOSC32 at VBAT LV level.
4:0	XOSCCALI	**GM calibration** Default: 4'b0111. 4'b0000 is suggested for the 2nd step EOSC_CALI = charging cap calibration

0A30 **RTC_POWERKEY1** **RTC_POWERKEY1 Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_POWERKEY1															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RTC_POWERKEY1	

0A32 RTC_POWERKEY2 RTC_POWERKEY2 Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_POWERKEY2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RTC_POWERKEY2	

0A34 RTC_PDN1 PDN1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_PDN1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RTC_PDN1	Spare registers for software to keep the power-on and power-off state information

0A36 RTC_PDN2 PDN2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_PDN2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RTC_PDN2	Spare registers for software to keep the power-on and power-off state information

0A38 RTC_SPAR0 Spare Register for Specific Purpose 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_SPAR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RTC_SPAR0	Reserved for specific purposes

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0A3A RTC_SPAR1 Spare Register for Specific Purpose 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_SPAR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RTC_SPAR1	Reserved for specific purposes

0A3C RTC_PROT Lock/Unlock Scheme to Prevent RTC Miswriting 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_PROT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

15:0	RTC_PROT	**The RTC write interface is protected by RTC_PROT.**
		Whether the RTC writing interface is enabled or not is decided by RTC_PROT contents. When RTC_POWERKEY1 & RTC_POWERKEY2 are not equal to the correct values, the RTC writing interface will always be enabled. When they match, perform the unlock flow to enable the writing interface.
		Unlock flow:
		1. *RTC_PROT=0x586a
		2. *RTC_WRTGR=1
		3. while(*RTC_BBPU & 0x40) {}; // Timeout period: 120usec
		4. *RTC_PROT=0x9136
		5. *RTC_WRTGR=1
		6. while(*RTC_BBPU & 0x40) {}; // Timeout period: 120usec
		Note: Always keep RTC in unlock state in power on mode. Once the normal RTC content writing is completed, do not modify the RTC_PROT content to lock RTC. The RTC_PROT contents will be cleared automatically when powered off immediately.

0A3E RTC_DIFF One-time Calibration Offset 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CALI_RD_SEL	K_EOSC32_RSV		POWER_DETECTED	RTC_DIFF											
Type	RW	RW		RO	RW											
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	CALI_RD_SEL	**Selects which RTC_CALI is to be read when read RTC_CALI register** 0: Normal RTC_CALI 1: K_EOSC32_RTC_CALI

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Bit(s)	Name	Description
14	K_EOSC32_RSV	**Reserved bit for EMB_K_EOSC32 mode**
12	POWER_DETECTED	**Read new power key match status**
11:0	RTC_DIFF	**Adjusts the internal counter of RTC** It takes effect once and returns to 0 when done. In some cases, observe the RTC is faster or slower than the standard. Changing RTC_TC_SEC is coarse and may cause alarm problems. RTC_DIFF provides a finer time unit. An internal 15-bit counter accumulates in each 32768Hz clock. Entering a non-zero value into RTC_DIFF will cause the internal RTC counter to increase or decrease RTC_DIFF when RTC_DIFF changes to 0 again. RTC_DIFF is in 2's complement. For example, if you fill in 0xfff in RTC_DIFF, the internal counter will decrease 1 when RTC_DIFF returns to 0. In other words, you can only use RTC_DIFF continuously if RTC_DIFF=0 now. Note: RTC_DIFF ranges from 0x800 (-2048) to 0x7fd (2045). 0x7ff and 0x7fe are forbidden to use.

0A40 **RTC_CALI** **Repeat Calibration Offset** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	K_EOSC32_OVERFLOW	CALI_WR_SEL	RTC_CALI													
Type	RW	RW	RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	K_EOSC32_OVERFLOW	**EOSC32 calibration overflow (EOSC32 RTC_CALI update result from PMU rtc_eosc_cali module overflow)** 0: Not overflow 1: Overflow
14	CALI_WR_SEL	**Enables EOSC32 Cali value write** Only takes effect in RTC_CALI write operation. 0: Normal RTC_CALI 1: K_EOSC32_RTC_CALI
13:0	RTC_CALI	**Repeat calibration scheme** RTC_CALI provides two types of calibration. (1) 7-bit calibration capability in 8-second duration, i.e. 5-bit calibration capability in each second. RTC_CALI is in 2's complement for user to adjust RTC increasing or decreasing. Due to RTC_CALI is revealed in 8 seconds, the resolution is less than a 1/32768 clock. Avg. resolution: 1/32768/8=3.81us Avg. adjust range: -0.244~0.240ms/sec in 2's complement: -0x40~0x3f (-64~63) (2) 14-bit calibration capability in 1-second duration in EMB_K_EOSC32 mode (K_EOSC32_RTC_CALI). This type of usage is with resolution 1/32768=30.52us.

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0A42 RTC_WRTGR Enable Transfers from Core to RTC in Queue 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WRTGR
Type																WO
Reset																0

Bit(s)	Name	Description
0	WRTGR	**Enables transfers from core to RTC** After modifying all the RTC registers that are to change, write 1 to RTC_WRTGR to trigger the transfer. The prior writing operations are queued at core power domain. The pending data will not be transferred to RTC domain until WRTGR=1. After WRTGR=1, the pending data will be transferred to RTC domain sequentially in order of register address, from low to high. For example: RTC_BBPU -> RTC_IRQ_EN -> RTC_CII_EN -> RTC_AL_MASK -> RTC_TC_SEC -> .... The CBUSY in RTC_BBPU is equal to 1 in writing process. You can observe CBUSY to determine when the transmission is completed.

0A44 RTC_CON Other RTC Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPSTA_RAW	GPI	GE8	GE4	GPU	GPEN	GSMT	GSR	GOE	GPO	F32KOB	CDBO		XOSC32_LPEN	EOSC32_LPEN	VBAT_LPSTA_RAW
Type	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
15	LPSTA_RAW	**Raw status of LP_STA** Re-initialize LPD to clear this bit. Note: This bit is always high before LPD initialization sequence after the first power-on.
14	GPI	**Input value of RTC_GPIO when GOE=0 (input mode)**
13	GE8	**Driving capability of RTC_GPIO**
12	GE4	**Driving capability of RTC_GPIO**
11	GPU	**Pull-up of RTC_GPIO**
10	GPEN	**Enables pull of RTC_GPIO** When GPEN=1, RTC_GPIO will be pull up if GPU=1; pull down if GPU=0.
9	GSMT	**SMT of RTC_GPIO** Control pin for Schmitt trigger circuit. 0: RTC_GPIO Schmitt trigger off 1: RTC_GPIO Schmitt trigger on
8	GSR	**SR of RTC_GPIO** Output slew rate control. High asserted. SR=0, slower slew. SR=1. 0: RTC_GPIO higher slew output 1: RTC_GPIO slower slew output
7	GOE	**OE of RTC_GPIO** 1'b0: RTC_GPIO is in input mode.

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Bit(s)	Name	Description
		1'b1: RTC_GPIO is in output mode.
6	GPO	**Output value of RTC_GPIO when OE=1 and COREDETB=0** To select to output pdn_flat_out signal or tick_sec to RTC_GPIO when OE=1 and COREDETB=1.
5	F32KOB	**Export 32.768kHz clock on RTC_GPIO in analog IO mode** 1'b0: Analog IO mode 1'b1: Digital IO mode
4	CDBO	**Exports signal on RTC_GPIO** 1'b0: Export GPO value 1'b1: When LPD_OPT=1, export LPDETB. When LPD_OPT=0 and GPO=0, export pdn_flat_out signal. When LPD_OPT=0 and GPO=1, export tick_sec.
2	XOSC32_LPEN	**Enables XOSC LPDETB function** LP initialization sequence to enable LPDETB: 1. Write XOSC32_LPEN = 1, LPRST = 0. Write RTC_WRTGR = 1. Wait for cbusy down. 2. Write XOSC32_LPEN = 1, LPRST = 1. Write RTC_WRTGR = 1. Wait for cbusy down. 3. Write XOSC32_LPEN = 1, LPRST = 0. Write RTC_WRTGR = 1. Wait for cbusy down. XOSC32 LPD will occur when 32k stops.
1	EOSC32_LPEN	**Enables EOSC LPDETB function** LP initialization sequence to enable LPDETB: 1. Write EOSC32_LPEN = 1, LPRST = 0. Write RTC_WRTGR = 1. Wait for cbusy down. 2. Write EOSC32_LPEN = 1, LPRST = 1. Write RTC_WRTGR = 1. Wait for cbusy down. 3. Write EOSC32_LPEN = 1, LPRST = 0. Write RTC_WRTGR = 1. Wait for cbusy down. EOSC32 LPD will occurs when VRTC~=1.25V.
0	VBAT_LPSTA_RAW	**Indicates the battery has been in LP state** When the embedded hardware mode is used, the flag also indicates that hardware has switched clock source from DCXO to EOSC32. Software needs to clear this bit for the next time use Note: VBAT LP state = VBAT < 2.5V (DDLO) 0: VBAT has not been in LP state. 1: VBAT has been in LP state.

0AC8	RTC_TC_SEC_SEC	Security RTC Seconds Time Counter Register	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TC_SECOND_SEC					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	TC_SECOND_SEC	**Second initial value for the time counter** Range: 0~59

0ACA	RTC_TC_MIN_SEC	Security RTC Minutes Time Counter Register	0000

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TC_MINUTE_SEC					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	TC_MINUTE_SEC	**Minute initial value for the time counter** Range: 0~59

0ACC	RTC_TC_HOU_SEC	Security RTC Hours Time Counter Register	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TC_HOUR_SEC				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TC_HOUR_SEC	**Hour initial value for the time counter** Range: 0~23

0ACE	RTC_TC_DOM_SEC	Security RTC Day-of-month Time Counter Register	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TC_DOM_SEC				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TC_DOM_SEC	**Day-of-month initial value for the time counter** The day-of-month maximum value depends on the leap year condition, i.e. 2 LSB of year time counter are 0.

0AD0	RTC_TC_DOW_SEC	Security RTC Day-of-week Time Counter Register	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														TC_DOW_SEC		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	TC_DOW_SEC	**Day-of-week initial value for the time counter** Range: 1~7

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0AD2 RTC_TC_MTH_SEC Security RTC Month Time Counter Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TC_MONTH_SEC			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TC_MONTH_SEC	**Month initial value for the time counter** Range: 1~12

0AD4 RTC_TC_YEA_SEC Security RTC Year Time Counter Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TC_YEAR_SEC						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	TC_YEAR_SEC	**Year initial value for the time counter** Range: 0~127 (2000~2127) Software can bias the year as multiples of 4 for the internal leap-year formula, e.g. 2000~2127, 1972~2099, 1904~2031. To simplify it, RTC hardware treats all 4-multiple as leap years. If the range you defined includes non-leap 4-multiple year (e.g. 2100), adjust to the correct date (e.g. change Feb. 29th, 2100 to Mar. 1st, 2100). It is suggested to bias the range larger than 1900 and less than 2100 to evade the manual adjustment, i.e. the bias values are suggested to be in the range of [-28,-96], which means (1972~2099) ~ (1904~2031). Formal leap formula: if year modulo 400 is 0 then leap else if year modulo 100 is 0 then no_leap else if year modulo 4 is 0 then leap else no_leap

0AD6 RTC_SEC_CK_PDN Security RTC Clock Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RTC_SEC_CK_PDN
Type																RW
Reset																0

Bit(s)	Name	Description
0	RTC_SEC_CK_PDN	**Security RTC clock control** 0: Turn off clock 1: Turn on clock

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0AD8	RTC_SEC_WRTGR	Enable Transfers from Core to Security RTC in Queue	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RTC_SEC_WRTGR
Type																WO
Reset																0

Bit(s)	Name	Description
0	RTC_SEC_WRTGR	**Enables the transfers from core to security RTC** After modifying all the RTC registers that is to change, write 1 to RTC_WRTGR to trigger the transfer. The prior writing operations are queued at core power domain. The pending data will not be transferred to RTC domain until WRTGR=1. After WRTGR=1, the pending data will be transferred to RTC domain sequentially in order of register address, from low to high. For example: RTC_TC_SEC_SEC -> RTC_TC_MIN_SEC -> RTC_TC_HOU_SEC ....

0B3A	BUCK_TOP_OC_CON0	BUCK_TOP OC Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_BUCK_VPA_OC_SDN_STATUS	RG_BUCK_VS2_OC_SDN_STATUS	RG_BUCK_VS1_OC_SDN_STATUS	RG_BUCK_VMODEM_OC_SDN_STATUS	RG_BUCK_VCORE_OC_SDN_STATUS	RG_BUCK_VPROC_OC_SDN_STATUS
Type											RO	RO	RO	RO	RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5	RG_BUCK_VPA_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
4	RG_BUCK_VS2_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
3	RG_BUCK_VS1_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
2	RG_BUCK_VMODEM_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
1	RG_BUCK_VCORE_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.

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Bit(s)	Name	Description
0	RG_BUCK_VPROC_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.

0B86 **BUCK_VPROC_CON0** **BUCK VPROC Control 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VPROC_LP	RG_BUCK_VPROC_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VPROC_LP	**Enters low power mode** Valid once RG_BUCK_VPROC_SW_OP_EN = 1'b1. 0: No LP 1: LP
0	RG_BUCK_VPROC_EN	**Enable control (SW mode)** Valid once RG_BUCK_VPROC_SW_OP_EN = 1'b1. 0: Off 1: On

0BA8 **BUCK_VPROC_ELR0** **BUCK_VPROC ELR 0 Register** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VPROC_VOSEL						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VPROC_VOSEL	**Selects VOUT in normal mode (SW mode)** Vout = 0.5V+6.25mV*code

0BC6 **BUCK_VCORE_CON0** **BUCK VCORE Control 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VCORE_LP	RG_BUCK_VCORE_EN
Type															RW	RW
Reset															0	1

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Bit(s)	Name	Description
1	RG_BUCK_VCORE_LP	**Enters low power mode** Valid once RG_BUCK_VCORE_SW_OP_EN = 1'b1. 0: No LP 1: LP
0	RG_BUCK_VCORE_EN	**Enable control (SW mode)** Valid once RG_BUCK_VCORE_SW_OP_EN = 1'b1. 0: Off 1: On

0BE8 **BUCK_VCORE_ELR0** **BUCK_VCORE ELR 0 Register** **0030**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VCORE_VOSEL						
Type										RW						
Reset										0	1	1	0	0	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VCORE_VOSEL	**Selects VOUT in normal mode (SW mode)** Vout = 0.5V+6.25mV*code

0C06 **BUCK_VMODEM_CON0** **BUCK VMODEM Control 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VMODEM_LP	RG_BUCK_VMODEM_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VMODEM_LP	**Enters low power mode** Valid once RG_BUCK_VMODEM_SW_OP_EN = 1'b1. 0: No LP 1: LP
0	RG_BUCK_VMODEM_EN	**Enable control (SW mode)** Valid once RG_BUCK_VMODEM_SW_OP_EN = 1'b1. 0: Off 1: On

0C30 **BUCK_VMODEM_ELR0** **BUCK_VMODEM ELR 0 Register** **0030**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VMODEM_VOSEL						

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Type										RW					
Reset										0	1	1	0	0	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VMODEM_VOSEL	**Selects VOUT in normal mode (SW mode)** Vout = 0.5V+6.25mV*code

0C46 BUCK_VS1_CON0 BUCK VS1 Control 0 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VS1_LP	RG_BUCK_VS1_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VS1_LP	**Enters low power mode** Valid once RG_BUCK_VS1_SW_OP_EN = 1'b1. 0: No LP 1: LP
0	RG_BUCK_VS1_EN	**Enable control (SW mode)** Valid once RG_BUCK_VS1_SW_OP_EN = 1'b1. 0: Off 1: On

0C6C BUCK_VS1_VOTER_CFG BUCK VS1 VOTER Configure 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VS1_VOTER_VOSEL						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VS1_VOTER_VOSEL	VS1 VOTER VOSEL

0C86 BUCK_VS2_CON0 BUCK VS2 Control 0 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VS2_LP	RG_BUCK_VS2_EN
Type															RW	RW
Reset															0	1

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Bit(s)	Name	Description
1	RG_BUCK_VS2_LP	**Enters low power mode** Valid once RG_BUCK_VS2_SW_OP_EN = 1'b1. 0: No LP 1: LP
0	RG_BUCK_VS2_EN	**Enable control (SW mode)** Valid once RG_BUCK_VS2_SW_OP_EN = 1'b1. 0: Off 1: On

0CAC **BUCK_VS2_VOTER_CFG** **BUCK VS2 VOTER Configure** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**RG_BUCK_VS2_VOTER_VOSEL**						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VS2_VOTER_VOSEL	VS2 VOTER VOSEL

0CC6 **BUCK_VPA_CON0** **BUCK VPA Control 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RG_BUCK_VPA_EN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_BUCK_VPA_EN	Enable control (SW mode)

0CC8 **BUCK_VPA_CON1** **BUCK VPA Control 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**RG_BUCK_VPA_VOSEL**					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	RG_BUCK_VPA_VOSEL	**Selects VOUT in normal mode (SW mode)** VOUT = 0.5V + 50mV*VOSEL

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0D18	VCORE_VPROC_ANA_CON5	VCORE_VPROC Control Register 5	0006

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RGS_VCORE_PREOC_STATUS	RGS_VPROC_OC_STATUS	RGS_VCORE_OC_STATUS			
Type											RO	RO	RO			
Reset											0	0	0			

Bit(s)	Name	Description
5	RGS_VCORE_PREOC_STATUS	**preoc status register** 0: No oc 1: preoc trigger
4	RGS_VPROC_OC_STATUS	**OC status** H: OC L: Normal operation
3	RGS_VCORE_OC_STATUS	**OC status** H: OC L: Normal operation

0D24	VCORE_VPROC_ANA_CON11	VCORE_VPROC Control Register 11	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_VPROC_NONAUDIBLE_EN	RG_VCORE_NONAUDIBLE_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_VPROC_NONAUDIBLE_EN	Enables PFM frequency > 25kHz
0	RG_VCORE_NONAUDIBLE_EN	Enables PFM frequency > 25kHz

0D34	VMODEM_ANA_CON7	VMODEM Control Register 7	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name			**RG_VMODEM_NONAUDIBLE_EN**									**RGS_VMODEM_OC_STATUS**				
Type			RW									RO				
Reset			0									0				

Bit(s)	Name	Description
13	RG_VMODEM_NONAUDIBLE_EN	**Enables PFM frequency > 25kHz**
4	RGS_VMODEM_OC_STATUS	**OC status** H: OC L: Normal operation

0D3E **VS1_ANA_CON4** VS1 Control Register 4 0600

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RGS_VS1_OC_STATUS**												
Type				RO												
Reset				0												

Bit(s)	Name	Description
12	RGS_VS1_OC_STATUS	**OC status** H: OC L: Normal operation

0D4A **VS2_ANA_CON4** VS2 Control Register 4 0600

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RGS_VS2_OC_STATUS**												
Type				RO												
Reset				0												

Bit(s)	Name	Description
12	RGS_VS2_OC_STATUS	**OC status** H: OC L: Normal operation

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0D58 **VPA_ANA_CON5** **VPA Control Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RGS_VPA_OC_STATUS
Type																RO
Reset																0

Bit(s)	Name	Description
0	RGS_VPA_OC_STATUS	**Over-current status** 0: No over-current occurs 1: Over-current occurs

0D6A **SMPS_ELR_7** **SMPS ELR 7 Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VOUTDET_EN													
Type			RW													
Reset			0													

Bit(s)	Name	Description
13	RG_VOUTDET_EN	Not used

0D8A **LDO_TOP_CLK_DCM_CON0** **LDO DCM Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_DCM_MODE
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_LDO_DCM_MODE	**LDO 1M/9M CG constraint mode** 1'b0: Old mode 1'b1: New mode (higher gated rate)

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0D8C	LDO_TOP_CLK_VIO28_CON0	LDO VIO28 Clock Gating Control Register 0	0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VIO28_OSC_SEL_DIS	RG_LDO_VIO28_CK_SW_EN	RG_LDO_VIO28_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VIO28_OSC_SEL_DIS	**Disables VIO28 OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VIO28_CK_SW_EN	**VIO28 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VIO28_CK_SW_MODE	**VIO28 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0D8E	LDO_TOP_CLK_VIO18_CON0	LDO VIO18 Clock Gating Control Register 0	0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VIO18_OSC_SEL_DIS	RG_LDO_VIO18_CK_SW_EN	RG_LDO_VIO18_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VIO18_OSC_SEL_DIS	**Disables VIO18 OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VIO18_CK_SW_EN	**VIO18 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VIO18_CK_SW_MODE	**VIO18 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

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0D90	LDO_TOP_CLK_VAUD28_CON0	LDO VAUD28 Clock Gating Control Register 0	0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VAUD28_OSC_SEL_DIS	RG_LDO_VAUD28_CK_SW_EN	RG_LDO_VAUD28_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VAUD28_OSC_SEL_DIS	**Disables VAUD28 OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VAUD28_CK_SW_EN	**VAUD28 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VAUD28_CK_SW_MODE	**VAUD28 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0D92	LDO_TOP_CLK_VDRAM_CON0	LDO VDRAM Clock Gating Control Register 0	0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VDRAM_OSC_SEL_DIS	RG_LDO_VDRAM_CK_SW_EN	RG_LDO_VDRAM_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VDRAM_OSC_SEL_DIS	**Disables VDRAM OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VDRAM_CK_SW_EN	**VDRAM clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VDRAM_CK_SW_MODE	**VDRAM clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

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0D94 | **LDO_TOP_CLK_VA12_CON0** | **LDO VA12 Clock Gating Control Register 0** | **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VA12_OSC_SEL_DIS	RG_LDO_VA12_CK_SW_EN	RG_LDO_VA12_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VA12_OSC_SEL_DIS	**Disables VA12 OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VA12_CK_SW_EN	**VA12 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VA12_CK_SW_MODE	**VA12 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0D96 | **LDO_TOP_CLK_VSRAM_PROC_CON0** | **LDO VSRAM_PROC Clock Gating Control Register 0** | **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VSRAM_PROC_OSC_SEL_DIS	RG_LDO_VSRAM_PROC_CK_SW_EN	RG_LDO_VSRAM_PROC_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VSRAM_PROC_OSC_SEL_DIS	**Disables VSRAM_PROC OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VSRAM_PROC_CK_SW_EN	**VSRAM_PROC clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VSRAM_PROC_CK_SW_MODE	**VSRAM_PROC clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

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0D98	LDO_TOP_CLK_VSRAM_OTHERS_CON0	LDO VSRAM_OTHERS Clock Gating Control Register 0	0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VSRAM_OTHERS_OSC_SEL_DIS	RG_LDO_VSRAM_OTHERS_CK_SW_EN	RG_LDO_VSRAM_OTHERS_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VSRAM_OTHERS_OSC_SEL_DIS	**Disables VSRAM_OTHERS OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VSRAM_OTHERS_CK_SW_EN	**VSRAM_OTHERS clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VSRAM_OTHERS_CK_SW_MODE	**VSRAM_OTHERS clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0D9A	LDO_TOP_CLK_VSRAM_GPU_CON0	LDO VSRAM_GPU Clock Gating Control Register 0	0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VSRAM_GPU_OSC_SEL_DIS	RG_LDO_VSRAM_GPU_CK_SW_EN	RG_LDO_VSRAM_GPU_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VSRAM_GPU_OSC_SEL_DIS	**Disables VSRAM_GPU OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VSRAM_GPU_CK_SW_EN	**VSRAM_GPU clock SW mode on/off control** 1'b0: Off

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Bit(s)	Name	Description
		1'b1: On
0	RG_LDO_VSRAM_GPU_CK_SW_MODE	**VSRAM_GPU clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0D9C LDO_TOP_CLK_VAUX18_CON0 — LDO VAUX18 Clock Gating Control Register 0 — 0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VAUX18_OSC_SEL_DIS	RG_LDO_VAUX18_CK_SW_EN	RG_LDO_VAUX18_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VAUX18_OSC_SEL_DIS	**Disables VAUX18 OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VAUX18_CK_SW_EN	**VAUX18 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VAUX18_CK_SW_MODE	**VAUX18 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0D9E LDO_TOP_CLK_VUSB_CON0 — LDO VUSB Clock Gating Control Register 0 — 0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VUSB_OSC_SEL_DIS	RG_LDO_VUSB_CK_SW_EN	RG_LDO_VUSB_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VUSB_OSC_SEL_DIS	**Disables VUSB OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable

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Bit(s)	Name	Description
1	RG_LDO_VUSB_CK_SW_EN	**VUSB clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VUSB_CK_SW_MODE	**VUSB clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DA0 LDO_TOP_CLK_VEMC_CON0 LDO VEMC Clock Gating Control Register 0 0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VEMC_OSC_SEL_DIS	RG_LDO_VEMC_CK_SW_EN	RG_LDO_VEMC_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VEMC_OSC_SEL_DIS	**Disables VEMC OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VEMC_CK_SW_EN	**VEMC clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VEMC_CK_SW_MODE	**VEMC clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DA2 LDO_TOP_CLK_VXO22_CON0 LDO VXO22 Clock Gating Control Register 0 0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VXO22_OSC_SEL_DIS	RG_LDO_VXO22_CK_SW_EN	RG_LDO_VXO22_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VXO22_OSC_SEL_DIS	**Disables VXO22 OSC_SEL HW mode to CLKCTL** 1'b0: Enable

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Bit(s)	Name	Description
		1'b1: Disable
1	RG_LDO_VXO22_CK_SW_EN	**VXO22 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VXO22_CK_SW_MODE	**VXO22 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DA4 **LDO_TOP_CLK_VSIM1_CON0** **LDO VSIM1 Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VSIM1_OSC_SEL_DIS	RG_LDO_VSIM1_CK_SW_EN	RG_LDO_VSIM1_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VSIM1_OSC_SEL_DIS	**Disables VSIM1 OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VSIM1_CK_SW_EN	**VSIM1 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VSIM1_CK_SW_MODE	**VSIM1 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DA6 **LDO_TOP_CLK_VSIM2_CON0** **LDO VSIM2 Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VSIM2_OSC_SEL_DIS	RG_LDO_VSIM2_CK_SW_EN	RG_LDO_VSIM2_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VSIM2_O	**Disables VSIM2 OSC_SEL HW mode to CLKCTL**

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Bit(s)	Name	Description
	SC_SEL_DIS	1'b0: Enable 1'b1: Disable
1	RG_LDO_VSIM2_CK_SW_EN	**VSIM2 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VSIM2_CK_SW_MODE	**VSIM2 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DA8 **LDO_TOP_CLK_VCAMD_CON0** **LDO VCAMD Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VCAMD_OSC_SEL_DIS	RG_LDO_VCAMD_CK_SW_EN	RG_LDO_VCAMD_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VCAMD_OSC_SEL_DIS	**Disables VCAMD OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VCAMD_CK_SW_EN	**VCAMD clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VCAMD_CK_SW_MODE	**VCAMD clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DAA **LDO_TOP_CLK_VCAMIO_CON0** **LDO VCAMIO Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VCAMIO_OSC_SEL_DIS	RG_LDO_VCAMIO_CK_SW_EN	RG_LDO_VCAMIO_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

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Bit(s)	Name	Description
2	RG_LDO_VCAMIO_OSC_SEL_DIS	**Disables VCAMIO OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VCAMIO_CK_SW_EN	**VCAMIO clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VCAMIO_CK_SW_MODE	**VCAMIO clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DAC **LDO_TOP_CLK_VMIPI_CON0** **LDO VMIPI Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VMIPI_OSC_SEL_DIS	RG_LDO_VMIPI_CK_SW_EN	RG_LDO_VMIPI_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VMIPI_OSC_SEL_DIS	**Disables VMIPI OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VMIPI_CK_SW_EN	**VMIPI clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VMIPI_CK_SW_MODE	**VMIPI clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DAE **LDO_TOP_CLK_VCN33_CON0** **LDO VCN33 Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VCN33_OSC_SEL_DIS	RG_LDO_VCN33_CK_SW_EN	RG_LDO_VCN33_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

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Bit(s)	Name	Description
2	RG_LDO_VCN33_OSC_SEL_DIS	**Disables VCN33 OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VCN33_CK_SW_EN	**VCN33 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VCN33_CK_SW_MODE	**VCN33 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DB0 **LDO_TOP_CLK_VCN18_CON0** **LDO VCN18 Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VCN18_OSC_SEL_DIS	RG_LDO_VCN18_CK_SW_EN	RG_LDO_VCN18_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VCN18_OSC_SEL_DIS	**Disables VCN18 OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VCN18_CK_SW_EN	**VCN18 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VCN18_CK_SW_MODE	**VCN18 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DB2 **LDO_TOP_CLK_VCN28_CON0** **LDO VCN28 Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VCN28_OSC_SEL_DIS	RG_LDO_VCN28_CK_SW_EN	RG_LDO_VCN28_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

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Bit(s)	Name	Description
2	RG_LDO_VCN28_OSC_SEL_DIS	**Disables VCN28 OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VCN28_CK_SW_EN	**VCN28 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VCN28_CK_SW_MODE	**VCN28 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DB4 **LDO_TOP_CLK_VIBR_CON0** **LDO VIBR Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VIBR_OSC_SEL_DIS	RG_LDO_VIBR_CK_SW_EN	RG_LDO_VIBR_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VIBR_OSC_SEL_DIS	**Disables VIBR OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VIBR_CK_SW_EN	**VIBR clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VIBR_CK_SW_MODE	**VIBR clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DB6 **LDO_TOP_CLK_VBIF28_CON0** **LDO VBIF28 Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VBIF28_OSC_SEL_DIS	RG_LDO_VBIF28_CK_SW_EN	RG_LDO_VBIF28_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

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Bit(s)	Name	Description
2	RG_LDO_VBIF28_OSC_SEL_DIS	**Disables VBIF28 OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VBIF28_CK_SW_EN	**VBIF28 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VBIF28_CK_SW_MODE	**VBIF28 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DB8 **LDO_TOP_CLK_VFE28_CON0** **LDO VFE28 Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VFE28_OSC_SEL_DIS	RG_LDO_VFE28_CK_SW_EN	RG_LDO_VFE28_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VFE28_OSC_SEL_DIS	**Disables VFE28 OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VFE28_CK_SW_EN	**VFE28 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VFE28_CK_SW_MODE	**VFE28 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DBA **LDO_TOP_CLK_VMCH_CON0** **LDO VMCH Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VMCH_OSC_SEL_DIS	RG_LDO_VMCH_CK_SW_EN	RG_LDO_VMCH_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

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Bit(s)	Name	Description
2	RG_LDO_VMCH_OSC_SEL_DIS	**Disables VMCH OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VMCH_CK_SW_EN	**VMCH clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VMCH_CK_SW_MODE	**VMCH clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DBC **LDO_TOP_CLK_VMC_CON0** **LDO VMC Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VMC_OSC_SEL_DIS	RG_LDO_VMC_CK_SW_EN	RG_LDO_VMC_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VMC_OSC_SEL_DIS	**Disables VMC OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VMC_CK_SW_EN	**VMC clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VMC_CK_SW_MODE	**VMC clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DBE **LDO_TOP_CLK_VRF18_CON0** **LDO VRF18 Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VRF18_OSC_SEL_DIS	RG_LDO_VRF18_CK_SW_EN	RG_LDO_VRF18_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

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Bit(s)	Name	Description
2	RG_LDO_VRF18_OSC_SEL_DIS	**Disables VRF18 OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VRF18_CK_SW_EN	**VRF18 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VRF18_CK_SW_MODE	**VRF18 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DC0 **LDO_TOP_CLK_VLDO28_CON0** **LDO VLDO28 Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VLDO28_OSC_SEL_DIS	RG_LDO_VLDO28_CK_SW_EN	RG_LDO_VLDO28_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VLDO28_OSC_SEL_DIS	**Disables VLDO28 OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VLDO28_CK_SW_EN	**VLDO28 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VLDO28_CK_SW_MODE	**VLDO28 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DC2 **LDO_TOP_CLK_VRF12_CON0** **LDO VRF12 Clock Gating Control Register 0** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VRF12_OSC_SEL_DIS	RG_LDO_VRF12_CK_SW_EN	RG_LDO_VRF12_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

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Bit(s)	Name	Description
2	RG_LDO_VRF12_OSC_SEL_DIS	**Disables VRF12 OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VRF12_CK_SW_EN	**VRF12 clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VRF12_CK_SW_MODE	**VRF12 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0DC4 LDO_TOP_CLK_VCAMA_CON0 LDO VCAMA Clock Gating Control Register 0 0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VCAMA_OSC_SEL_DIS	RG_LDO_VCAMA_CK_SW_EN	RG_LDO_VCAMA_CK_SW_MODE
Type														RW	RW	RW
Reset														0	1	1

Bit(s)	Name	Description
2	RG_LDO_VCAMA_OSC_SEL_DIS	**Disables VCAMA OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
1	RG_LDO_VCAMA_CK_SW_EN	**VCAMA clock SW mode on/off control** 1'b0: Off 1'b1: On
0	RG_LDO_VCAMA_CK_SW_MODE	**VCAMA clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

0E18 LDO_VXO22_CON1 LDO VXO22 Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VXO22_EN							DA_VXO22_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VXO22_EN	**VXO22 enable status** 1'b0: Disable

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Bit(s)	Name	Description
		1'b1: Enable
8	DA_VXO22_MODE	**VXO22 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0E2C **LDO_VA12_CON1** **LDO VA12 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VA12_EN							DA_VA12_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VA12_EN	**VA12 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VA12_MODE	**VA12 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0E40 **LDO_VAUX18_CON1** **LDO VAUX18 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VAUX18_EN							DA_VAUX18_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VAUX18_EN	**VAUX18 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VAUX18_MODE	**VAUX18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0E54 **LDO_VAUD28_CON1** **LDO VAUD28 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VAUD28							DA_VAUD28								

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	_EN							_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VAUD28_EN	**VAUD28 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VAUD28_MODE	**VAUD28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0E68 LDO_VIO28_CON1 LDO VIO28 Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VIO28_EN							DA_VIO28_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VIO28_EN	**VIO28 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VIO28_MODE	**VIO28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0E7C LDO_VIO18_CON1 LDO VIO18 Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VIO18_EN							DA_VIO18_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VIO18_EN	**VIO18 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VIO18_MODE	**VIO18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

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0E90 **LDO_VDRAM_CON1** **LDO VDRAM Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VDRAM_EN							DA_VDRAM_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VDRAM_EN	**VDRAM enable status** 1'b0: Disable 1'b1: Enable
8	DA_VDRAM_MODE	**VDRAM low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0EA4 **LDO_VEMC_CON1** **LDO VEMC Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VEMC_EN							DA_VEMC_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VEMC_EN	**VEMC enable status** 1'b1: enable 1'b0: disable
8	DA_VEMC_MODE	**VEMC low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0F0A **LDO_VFE28_CON0** **LDO VFE28 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VFE28_LP	RG_LDO_VFE28_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VFE28_LP	**Enters low power mode** Valid once RG_LDO_VFE28_SW_OP_EN = 1'b1.

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Bit(s)	Name	Description
		1'b0: No LP 1'b1: LP
0	RG_LDO_VFE28_EN	**Enable control (SW mode)** Valid once RG_LDO_VFE28_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

0F18 **LDO_VFE28_CON1** **LDO VFE28 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VFE28_EN							DA_VFE28_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VFE28_EN	**VFE28 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VFE28_MODE	**VFE28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0F1E **LDO_VRF18_CON0** **LDO VRF18 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VRF18_LP	RG_LDO_VRF18_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VRF18_LP	**Enters low power mode** Valid once RG_LDO_VRF18_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VRF18_EN	**Enable control (SW mode)** Valid once RG_LDO_VRF18_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

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0F2C LDO_VRF18_CON1 LDO VRF18 Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VRF18_EN							DA_VRF18_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VRF18_EN	**VRF18 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VRF18_MODE	**VRF18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0F32 LDO_VRF12_CON0 LDO VRF12 Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VRF12_LP	RG_LDO_VRF12_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VRF12_LP	**Enters low power mode** Valid once RG_LDO_VRF12_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VRF12_EN	**Enable control (SW mode)** Valid once RG_LDO_VRF12_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

0F40 LDO_VRF12_CON1 LDO VRF12 Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VRF12_EN							DA_VRF12_MODE								
Type	RO							RO								
Reset	0							0								

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Bit(s)	Name	Description
15	DA_VRF12_EN	**VRF12 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VRF12_MODE	**VRF12 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0F46 LDO_VMIPI_CON0 LDO VMIPI Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VMIPI_LP	RG_LDO_VMIPI_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VMIPI_LP	**Enters low power mode** Valid once RG_LDO_VMIPI_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VMIPI_EN	**Enable control (SW mode)** Valid once RG_LDO_VMIPI_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

0F54 LDO_VMIPI_CON1 LDO VMIPI Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VMIPI_EN							DA_VMIPI_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VMIPI_EN	**VMIPI enable status** 1'b0: Disable 1'b1: Enable
8	DA_VMIPI_MODE	**VMIPI low power mode status** 1'b0: Normal mode 1'b1: Low power mode

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0F5A **LDO_VCN18_CON0** **LDO VCN18 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCN18_LP	RG_LDO_VCN18_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCN18_LP	**Enters low power mode** Valid once RG_LDO_VCN18_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VCN18_EN	**Enable control (SW mode)** Valid once RG_LDO_VCN18_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

0F68 **LDO_VCN18_CON1** **LDO VCN18 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VCN18_EN							DA_VCN18_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VCN18_EN	**VCN18 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VCN18_MODE	**VCN18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0F6E **LDO_VCAMA_CON0** **LDO VCAMA Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCAMA_LP	RG_LDO_VCAMA_EN
Type															RW	RW
Reset															0	0

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Bit(s)	Name	Description
1	RG_LDO_VCAMA_LP	**Enters low power mode** Valid once RG_LDO_VCAMA_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VCAMA_EN	**Enable control (SW mode)** Valid once RG_LDO_VCAMA_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

0F7C **LDO_VCAMA_CON1** **LDO VCAMA Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VCAMA_EN							DA_VCAMA_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VCAMA_EN	**VCAMA enable status** 1'b0: Disable 1'b1: Enable
8	DA_VCAMA_MODE	**VCAMA low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0F82 **LDO_VCAMD_CON0** **LDO VCAMD Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCAMD_LP	RG_LDO_VCAMD_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCAMD_LP	**Enters low power mode** Valid once RG_LDO_VCAMD_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VCAMD_EN	**Enable control (SW mode)** Valid once RG_LDO_VCAMD_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

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0F90 **LDO_VCAMD_CON1** **LDO VCAMD Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VCAMD_EN							DA_VCAMD_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VCAMD_EN	**VCAMD enable status** 1'b0: Disable 1'b1: Enable
8	DA_VCAMD_MODE	**VCAMD low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0F96 **LDO_VCAMIO_CON0** **LDO VCAMIO Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCAMIO_LP	RG_LDO_VCAMIO_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCAMIO_LP	**Enters low power mode** Valid once RG_LDO_VCAMIO_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VCAMIO_EN	**Enable control (SW mode)** Valid once RG_LDO_VCAMIO_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

0FA4 **LDO_VCAMIO_CON1** **LDO VCAMIO Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VCAMIO_EN							DA_VCAMIO_MODE								
Type	RO							RO								
Reset	0							0								

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Bit(s)	Name	Description
15	DA_VCAMIO_EN	**VCAMIO enable status** 1'b0: Disable 1'b1: Enable
8	DA_VCAMIO_MODE	**VCAMIO low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0FAA **LDO_VMC_CON0** **LDO VMC Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VMC_LP	RG_LDO_VMC_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VMC_LP	**Enters low power mode** Valid once RG_LDO_VMC_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VMC_EN	**Enable control (SW mode)** Valid once RG_LDO_VMC_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

0FB8 **LDO_VMC_CON1** **LDO VMC Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VMC_EN							DA_VMC_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VMC_EN	**VMC enable status** 1'b0: Disable 1'b1: Enable
8	DA_VMC_MODE	**VMC low power mode status** 1'b0: Normal mode 1'b1: Low power mode

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0FBE **LDO_VMCH_CON0** **LDO VMCH Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VMCH_LP	RG_LDO_VMCH_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VMCH_LP	**Enters low power mode** Valid once RG_LDO_VMCH_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VMCH_EN	**Enable control (SW mode)** Valid once RG_LDO_VMCH_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

0FCC **LDO_VMCH_CON1** **LDO VMCH Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VMCH_EN							DA_VMCH_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VMCH_EN	**VMCH enable status** 1'b0: Disable 1'b1: Enable
8	DA_VMCH_MODE	**VMCH low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0FD0 **LDO_VMCH_CON3** **LDO VMCH Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_LDO_VMCH_DUMMY_LOAD						
Type										RW						
Reset										0	0					

Bit(s)	Name	Description
6:5	RG_LDO_VMCH_D	**VMCH dummy load selection**

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Bit(s)	Name	Description
	UMMY_LOAD	2'b00: 0A dummy load 2'b01: 100uA dummy load 2'b10: 1mA dummy load 2'b11: 1.1mA dummy load

0FD2 **LDO_VSIM1_CON0** **LDO VSIM1 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VSIM1_LP	RG_LDO_VSIM1_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VSIM1_LP	**Enters low power mode** Valid once RG_LDO_VSIM1_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VSIM1_EN	**Enable control (SW mode)** Valid once RG_LDO_VSIM1_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

0FE0 **LDO_VSIM1_CON1** **LDO VSIM1 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VSIM1_EN							DA_VSIM1_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VSIM1_EN	**VSIM1 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VSIM1_MODE	**VSIM1 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0FE6 **LDO_VSIM2_CON0** **LDO VSIM2 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name															**RG_LDO_VSIM2_LP**	**RG_LDO_VSIM2_EN**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VSIM2_LP	**Enters low power mode** Valid once RG_LDO_VSIM2_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VSIM2_EN	**Enable control (SW mode)** Valid once RG_LDO_VSIM2_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

0FF4 <u>LDO_VSIM2_CON1</u> LDO VSIM2 Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_VSIM2_EN**							**DA_VSIM2_MODE**								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VSIM2_EN	**VSIM2 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VSIM2_MODE	**VSIM2 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

100A <u>LDO_VIBR_CON0</u> LDO VIBR Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**RG_LDO_VIBR_LP**	**RG_LDO_VIBR_EN**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VIBR_LP	**Enters low power mode** Valid once RG_LDO_VIBR_SW_OP_EN = 1'b1. 1'b0: No LP

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Bit(s)	Name	Description
		1'b1: LP
0	RG_LDO_VIBR_EN	**Enable control (SW mode)** Valid once RG_LDO_VIBR_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

1018 **LDO_VIBR_CON1** **LDO VIBR Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VIBR_EN							DA_VIBR_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VIBR_EN	**VIBR enable status** 1'b0: Disable 1'b1: Enable
8	DA_VIBR_MODE	**VIBR low power mode status** 1'b0: Normal mode 1'b1: Low power mode

101E **LDO_VBIF28_CON0** **LDO VBIF28 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VBIF28_LP	RG_LDO_VBIF28_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VBIF28_LP	**Enters low power mode** Valid once RG_LDO_VBIF28_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VBIF28_EN	**Enable control (SW mode)** Valid once RG_LDO_VBIF28_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

102C **LDO_VBIF28_CON1** **LDO VBIF28 Control Register 1** **0200**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VBIF28_EN							DA_VBIF28_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VBIF28_EN	**VBIF28 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VBIF28_MODE	**VBIF28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

104A LDO_VCN33_CON0_0 LDO VCN33 BT Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCN33_LP	RG_LDO_VCN33_EN_0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCN33_LP	**Enters low power mode** Valid once RG_LDO_VCN33_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VCN33_EN_0	**Enable control (SW mode)(BT)** Valid once RG_LDO_VCN33_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

1058 LDO_VCN33_CON0_1 LDO VCN33 WiFi Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCN33_EN_1
Type																RW
Reset																0

Bit(s)	Name	Description

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Bit(s)	Name	Description
0	RG_LDO_VCN33_EN_1	**Enable control (SW mode)(WIFI)** Valid once RG_LDO_VCN33_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

105A **LDO_VCN33_CON1** **LDO VCN33 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VCN33_EN							DA_VCN33_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VCN33_EN	**VCN33 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VCN33_MODE	**VCN33 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1060 **LDO_VLDO28_CON0_0** **LDO VLDO28 AF Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VLDO28_LP	RG_LDO_VLDO28_EN_0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VLDO28_LP	**Enters low power mode** Valid once RG_LDO_VLDO28_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VLDO28_EN_0	**Enable control (SW mode)(AF)** Valid once RG_LDO_VLDO28_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

106E **LDO_VLDO28_CON0_1** **LDO VLDO28 TP Control Register 0** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VLDO28_EN_1
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_LDO_VLDO28_EN_1	**Enable control (SW mode)(TP)** Valid once RG_LDO_VLDO28_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

1070 **LDO_VLDO28_CON1** **LDO VLDO28 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VLDO28_EN							DA_VLDO28_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VLDO28_EN	**VLDO28 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VLDO28_MODE	**VLDO28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1076 **LDO_VUSB_CON0_0** **LDO VUSB 0 Control Register 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VUSB_LP	RG_LDO_VUSB_EN_0
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_LDO_VUSB_LP	**Enters low power mode** Valid once RG_LDO_VUSB_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP

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Bit(s)	Name	Description
0	RG_LDO_VUSB_EN_0	**Enable control (SW mode)** Valid once RG_LDO_VUSB_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

1084 **LDO_VUSB_CON0_1** **LDO VUSB 1 Control Register 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VUSB_EN_1
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VUSB_EN_1	**Enable control (SW mode)** Valid once RG_LDO_VUSB_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

1086 **LDO_VUSB_CON1** **LDO VUSB Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VUSB_EN							DA_VUSB_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VUSB_EN	**VUSB enable status** 1'b0: Disable 1'b1: Enable
8	DA_VUSB_MODE	**VUSB low power mode status** 1'b0: Normal mode 1'b1: Low power mode

10CA **LDO_VCN28_CON0** **LDO VCN28 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCN28_LP	RG_LDO_VCN28_EN

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Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCN28_LP	**Enters low power mode** Valid once RG_LDO_VCN28_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VCN28_EN	**Enable control (SW mode)** Valid once RG_LDO_VCN28_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

10D8 **LDO_VCN28_CON1** **LDO VCN28 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_VCN28_EN**							**DA_VCN28_MODE**								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VCN28_EN	**VCN28 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VCN28_MODE	**VCN28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

111E **LDO_VSRAM_PROC_CON3** **LDO VSRAM_PROC Control Register 3** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**DA_VSRAM_PROC_MODE**								
Type								RO								
Reset								0								

Bit(s)	Name	Description
8	DA_VSRAM_PROC_MODE	**VSRAM_PROC low power mode status** 1'b0: Normal mode 1'b1: Low power mode

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1126	LDO_VSRAM_PROC_DBG1	LDO VSRAM_PROC DEBUG 1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DA_VSRAM_PROC_EN
Type																RO
Reset																0

Bit(s)	Name	Description
0	DA_VSRAM_PROC_EN	VSRAM_PROC enable status

113C	LDO_VSRAM_OTHERS_CON3	LDO VSRAM_OTHERS Control Register 3	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DA_VSRAM_OTHERS_MODE								
Type								RO								
Reset								0								

Bit(s)	Name	Description
8	DA_VSRAM_OTHERS_MODE	**VSRAM_OTHERS low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1144	LDO_VSRAM_OTHERS_DBG1	LDO VSRAM_OTHERS DEBUG 1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DA_VSRAM_OTHERS_EN
Type																RO
Reset																0

Bit(s)	Name	Description
0	DA_VSRAM_OTHERS_EN	VSRAM_OTHERS enable status

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115A LDO_VSRAM_GPU_CON3 — LDO VSRAM_GPU Control Register 3 — 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DA_VSRAM_GPU_MODE								
Type								RO								
Reset								0								

Bit(s)	Name	Description
8	DA_VSRAM_GPU_MODE	**VSRAM_GPU low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1162 LDO_VSRAM_GPU_DBG1 — LDO VSRAM_GPU DEBUG 1 — 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DA_VSRAM_GPU_EN
Type																RO
Reset																0

Bit(s)	Name	Description
0	DA_VSRAM_GPU_EN	VSRAM_GPU enable status

1188 LDO_VSRAM_CON0 — LDO VSRAM CONTROL 0 — 4060

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_LDO_VSRAM_OTHERS_VOSEL_RO														
Type		RO														
Reset		1	0	0	0	0	0	0								

Bit(s)	Name	Description
14:8	RG_LDO_VSRAM_OTHERS_VOSEL_RO	**VOUT selection in normal mode (SW mode)** Vout = 0.5V+6.25mV*code

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120A **VRTC_CON0** **VRTC Control Register 0** **8002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VRTC_EN														RG_VRTC_EN	
Type	RO														RW	
Reset	1														1	

Bit(s)	Name	Description
15	DA_VRTC_EN	**VRTC enable status**
1	RG_VRTC_EN	**Enables VRTC** 1'b0: Disable 1'b1: Enable

1246 **VCAMA_ANA_CON0** **VCAMA Control Register 0** **0A00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCAMA_VOSEL								RG_VCAMA_VOCAL			
Type					RW								RW			
Reset					1	0	1	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCAMA_VOSEL	**Selects output voltage** 4'b0000: 1.8V 4'b0111: 2.5V 4'b1010: 2.8V
3:0	RG_VCAMA_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

124A **VFE28_ANA_CON0** **VFE28 Control Register 0** **0A00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VFE28_VOSEL								RG_VFE28_VOCAL			
Type					RW								RW			
Reset					1	0	1	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VFE28_VOSEL	**Selects output voltage** 4'b1010: 2.8V

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Bit(s)	Name	Description
3:0	RG_VFE28_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

124E **VCN28_ANA_CON0** **VCN28 Control Register 0** **0A00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCN28_VOSEL								RG_VCN28_VOCAL			
Type					RW								RW			
Reset					1	0	1	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCN28_VOSEL	**Selects output voltage** 4'b1010: 2.8V
3:0	RG_VCN28_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1252 **VBIF28_ANA_CON0** **VBIF28 Control Register 0** **0A00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VBIF28_VOSEL								RG_VBIF28_VOCAL			
Type					RW								RW			
Reset					1	0	1	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VBIF28_VOSEL	**Selects output voltage** 4'b1010: 2.8V
3:0	RG_VBIF28_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV

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Bit(s)	Name	Description
		4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1262 VCN33_ANA_CON0 VCN33 Control Register 0 0D00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCN33_VOSEL								RG_VCN33_VOCAL			
Type					RW								RW			
Reset					1	1	0	1					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCN33_VOSEL	**Selects output voltage** 4'b1101: 3.3V 4'b1110: 3.4V 4'b1111: 3.5V
3:0	RG_VCN33_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

126E VLDO28_ANA_CON0 VLDO28 Control Register 0 0900

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VLDO28_VOSEL								RG_VLDO28_VOCAL			
Type					RW								RW			
Reset					1	0	0	1					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VLDO28_VOSEL	**Selects output voltage** 4'b1001: 2.8V 4'b1011: 3.0V
3:0	RG_VLDO28_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV

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Bit(s)	Name	Description
		4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1276 **VIBR_ANA_CON0** **VIBR Control Register 0** **0900**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VIBR_VOSEL								RG_VIBR_VOCAL			
Type					RW								RW			
Reset					1	0	0	1					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VIBR_VOSEL	**Selects output voltage** 4'b0000: 1.2V 4'b0001: 1.3V 4'b0010: 1.5V 4'b0100: 1.8V 4'b1001: 2.8V 4'b1010: 2.9V 4'b1011: 3.0V 4'b1101: 3.3V
3:0	RG_VIBR_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

127A **VSIM1_ANA_CON0** **VSIM1 Control Register 0** **0406**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VSIM1_VOSEL								RG_VSIM1_VOCAL			
Type					RW								RW			
Reset					0	1	0	0					0	1	1	0

Bit(s)	Name	Description
11:8	RG_VSIM1_VOSEL	**Selects output voltage** 4'b0011: 1.7V 4'b0100: 1.8V 4'b1000: 2.7V 4'b1011: 3.0V 4'b1100: 3.1V

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Bit(s)	Name	Description
3:0	RG_VSIM1_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

127E **VSIM2_ANA_CON0** **VSIM2 Control Register 0** **0406**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VSIM2_VOSEL								RG_VSIM2_VOCAL			
Type					RW								RW			
Reset					0	1	0	0					0	1	1	0

Bit(s)	Name	Description
11:8	RG_VSIM2_VOSEL	**Selects output voltage** 4'b0011: 1.7V 4'b0100: 1.8V 4'b1000: 2.7V 4'b1011: 3.0V 4'b1100: 3.1V
3:0	RG_VSIM2_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1282 **VMCH_ANA_CON0** **VMCH Control Register 0** **0B00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VMCH_VOSEL								RG_VMCH_VOCAL			
Type					RW								RW			
Reset					1	0	1	1					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VMCH_VOSEL	**Selects output voltage** 4'b1010: 2.9V 4'b1011: 3.0V

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Bit(s)	Name	Description
		4'b1101: 3.3V
3:0	RG_VMCH_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1286 VMC_ANA_CON0 VMC Control Register 0 0B00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VMC_VOSEL								RG_VMC_VOCAL			
Type					RW								RW			
Reset					1	0	1	1					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VMC_VOSEL	**Selects output voltage** 4'b0100: 1.8V 4'b1010: 2.9V 4'b1011: 3.0V 4'b1101: 3.3V
3:0	RG_VMC_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

128A VCAMIO_ANA_CON0 VCAMIO Control Register 0 0C00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCAMIO_VOSEL								RG_VCAMIO_VOCAL			
Type					RW								RW			
Reset					1	1	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCAMIO_VOSEL	**Selects output voltage** 4'b1100: 1.8V

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Bit(s)	Name	Description
3:0	RG_VCAMIO_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

128E **VCN18_ANA_CON0** **VCN18 Control Register 0** **0C00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCN18_VOSEL								RG_VCN18_VOCAL			
Type					RW								RW			
Reset					1	1	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCN18_VOSEL	**Selects output voltage** 4'b1100: 1.8V
3:0	RG_VCN18_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1292 **VRF18_ANA_CON0** **VRF18 Control Register 0** **0700**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VRF18_VOSEL								RG_VRF18_VOCAL			
Type					RW								RW			
Reset					0	1	1	1					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VRF18_VOSEL	**Selects output voltage** 4'b0111: 1.81V
3:0	RG_VRF18_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV

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Bit(s)	Name	Description
		4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

129A **VMIPI_ANA_CON0** **VMIPI Control Register 0** **0C00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VMIPI_VOSEL								RG_VMIPI_VOCAL			
Type					RW								RW			
Reset					1	1	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VMIPI_VOSEL	**Selects output voltage** 4'b1011: 1.7V 4'b1100: 1.8V
3:0	RG_VMIPI_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

12A2 **VRF12_ANA_CON0** **VRF12 Control Register 0** **0300**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VRF12_VOSEL								RG_VRF12_VOCAL			
Type					RW								RW			
Reset					0	0	1	1					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VRF12_VOSEL	**Selects output voltage** 4'b0011: 1.2V
3:0	RG_VRF12_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV

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Bit(s)	Name	Description
		4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

12B0 **CAMD_ANA_CON0** **CAMD Control Register 0** **0600**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCAMD_VOSEL								RG_VCAMD_VOCAL			
Type					RW								RW			
Reset					0	1	1	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCAMD_VOSEL	**Selects output voltage** 4'b0100: 1.0V 4'b0101: 1.1V 4'b0110: 1.2V 4'b0111: 1.3V 4'b1001: 1.5V 4'b1100: 1.8V
3:0	RG_VCAMD_VOCAL	**Output voltage calibration** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

134E **XPP_TOP_CKPDN_CON0** **XPP_TOP_CKPDN Control Register 0** **039F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_XPP_RSV1_CK_PDN	RG_XPP_RSV0_CK_PDN								
Type							RW	RW								
Reset							1	1								

Bit(s)	Name	Description
9	RG_XPP_RSV1_CK_PDN	**Powers down XPP_RSV1_CK** 0: Power on 1: Power down
8	RG_XPP_RSV0_CK	**Powers down XPP_RSV0_CK**

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Bit(s)	Name	Description
	_PDN	0: Power on 1: Power down

1350	XPP_TOP_CKPDN_CON0_SET	XPP_TOP_CKPDN_CON0 Register SET	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XPP_TOP_CKPDN_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XPP_TOP_CKPDN_CON0_SET	**Sets up XPP_TOP_CKPDN_CON0** 1'b0: Not set 1'b1: Set

1352	XPP_TOP_CKPDN_CON0_CLR	XPP_TOP_CKPDN_CON0 Register CLR	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XPP_TOP_CKPDN_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XPP_TOP_CKPDN_CON0_CLR	**Clears XPP_TOP_CKPDN_CON0** 1'b0: Not clear 1'b1: Clear

1354	XPP_TOP_CKSEL_CON0	XPP_TOP_CKSEL Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													XPP_CKSEL_CON0_RSV			
Type													RW			
Reset													0	0		

Bit(s)	Name	Description
3:2	XPP_CKSEL_CON0_RSV	

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1356 **XPP_TOP_CKSEL_CON0_SET** **XPP_TOP_CKSEL_CON0 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XPP_TOP_CKSEL_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XPP_TOP_CKSEL_CON0_SET	**Sets up XPP_TOP_CKSEL_CON0** 1'b0: Not set 1'b1: Set

1358 **XPP_TOP_CKSEL_CON0_CLR** **XPP_TOP_CKSEL_CON0 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XPP_TOP_CKSEL_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XPP_TOP_CKSEL_CON0_CLR	**Clears XPP_TOP_CKSEL_CON0** 1'b0: Not clear 1'b1: Clear

135A **XPP_TOP_CKDIVSEL_CON0** **XPP_TOP_CKDIVSEL Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																XPP_CKDIVSEL_CON0_RSV
Type																RW
Reset																0

Bit(s)	Name	Description
0	XPP_CKDIVSEL_CON0_RSV	

135C **XPP_TOP_CKDIVSEL_CON0_SET** **XPP_TOP_CKDIVSEL_CON0 Register SET** **0000**

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135C	XPP_TOP_CKDIVSEL_CONo_SET	XPP_TOP_CKDIVSEL_CONo Register SET	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XPP_TOP_CKDIVSEL_CONo_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XPP_TOP_CKDIVSEL_CONo_SET	**Sets up XPP_TOP_CKDIVSEL_CONo** 1'b0: Not set 1'b1: Set

135E	XPP_TOP_CKDIVSEL_CONo_CLR	XPP_TOP_CKDIVSEL_CONo Register CLR	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XPP_TOP_CKDIVSEL_CONo_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XPP_TOP_CKDIVSEL_CONo_CLR	**Clears XPP_TOP_CKDIVSEL_CONo** 1'b0: Not clear 1'b1: Clear

1360	XPP_TOP_CKHWEN_CONo	XPP_TOP_CKHWEN Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																XPP_CKHWEN_CONo_RSV
Type																RW
Reset																0

Bit(s)	Name	Description
0	XPP_CKHWEN_CONo_RSV	

1362	XPP_TOP_CKHWEN_CONo_SET	XPP_TOP_CKHWEN_CONo Register SET	0000

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1362	XPP_TOP_CKHWEN_CON0_SET	XPP_TOP_CKHWEN_CON0 Register SET	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XPP_TOP_CKHWEN_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XPP_TOP_CKHWEN_CON0_SET	**Sets up XPP_TOP_CKHWEN_CON0** 1'b0: Not set 1'b1: Set

1364	XPP_TOP_CKHWEN_CON0_CLR	XPP_TOP_CKHWEN_CON0 Register CLR	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XPP_TOP_CKHWEN_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XPP_TOP_CKHWEN_CON0_CLR	**Clears XPP_TOP_CKHWEN_CON0** 1'b0: Not clear 1'b1: Clear

154A	AUD_TOP_CKPDN_CON0	AUDIO CLK Power Down Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_AUDNCP_CK_PDN	RG_ZCD13M_CK_PDN			RG_AUDIF_CK_PDN	RG_AUD_CK_PDN	RG_ACCDET_CK_PDN
Type										RW	RW			RW	RW	RW
Reset										0	0			0	0	0

Bit(s)	Name	Description
6	RG_AUDNCP_CK_PDN	**Powers down AUDNCP_CK** 0: Power on 1: Power down
5	RG_ZCD13M_CK_PDN	**Powers down ZCD13M_CK** 0: Power on 1: Power down
2	RG_AUDIF_CK_PDN	**Powers down AUDIF_CK** 0: Power on 1: Power down

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Bit(s)	Name	Description
1	RG_AUD_CK_PDN	**Powers down AUD_CK** 0: Power on 1: Power down
0	RG_ACCDET_CK_PDN	**Powers down ACCDET_CK** 0: Power on 1: Power down

154C **AUD_TOP_CKSEL_CON0** **AUDIO CKSEL Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_AUDIF_CK_CKSEL	RG_AUD_CK_CKSEL		
Type													RW	RW		
Reset													0	0		

Bit(s)	Name	Description
3	RG_AUDIF_CK_CKSEL	**Selects AUDIF_CK clock** 1'b0: R_AUD_CLK_MOSI 1'b1: R_AUD26M_CK
2	RG_AUD_CK_CKSEL	**Selects AUD_CK clock** 1'b0: R_AUD26M_CK 1'b1: R_AUD_CLK_MOSI

1566 **AUDNCP_CLKDIV_CON0** **AUDNCP_CLKDIV Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DIVCKS_CHG
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_DIVCKS_CHG	**Divider change enable signal** Toggle this bit will change ncp div value to ncp counters.

1568 **AUDNCP_CLKDIV_CON1** **AUDNCP_CLKDIV Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DIVCKS

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1568 **AUDNCP_CLKDIV_CON1** **AUDNCP_CLKDIV Control Register 1** **0000**

																_ON
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_DIVCKS_ON	**Divider enable bit** Set to 1'b1 to enable ncp.

156A **AUDNCP_CLKDIV_CON2** **AUDNCP_CLKDIV Control Register 2** **002C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**RG_DIVCKS_PRG**								
Type								RW								
Reset								0	0	0	1	0	1	1	0	0

Bit(s)	Name	Description
8:0	RG_DIVCKS_PRG	ncp divider program register

156C **AUDNCP_CLKDIV_CON3** **AUDNCP_CLKDIV Control Register 3** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RG_DIVCKS_PWD_NCP**
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_DIVCKS_PWD_NCP	power do

156E **AUDNCP_CLKDIV_CON4** **AUDNCP_CLKDIV Control Register 4** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**RG_DIVCKS_PWD_NCP_ST_SEL**	
Type															RW	
Reset															1	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
1:0	RG_DIVCKS_PWD_NCP_ST_SEL	**Selects ncp soft start time** 2'b00: 50us 2'b01: 100us 2'b10: 150us 2'b11: 200us

1570	AUD_TOP_MON_CON0	AUD_TOP_MON Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUD_CLK_INT_MON_FLAG_EN	RG_AUD_CLK_INT_MON_FLAG_SEL										
Type					RW	RW										
Reset					0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
11	RG_AUD_CLK_INT_MON_FLAG_EN	Enables accdet monitor flag
10:3	RG_AUD_CLK_INT_MON_FLAG_SEL	Selects accdet monitor flag

1586	AFE_UL_DL_CON0	Audio UL and DL Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_ul_lr_swap	afe_dl_lr_swap														afe_on
Type	RW	RW														RW
Reset	0	0														0

Bit(s)	Name	Description
15	afe_ul_lr_swap	Swaps audio UL L/R channel before UL SRC
14	afe_dl_lr_swap	Swaps audio DL L/R channel before DAC FIFO
0	afe_on	Turns on audio UL and DL

1588	AFE_DL_SRC2_CON0_L	AFE_DL_SRC2 Control Register 0 Low Part	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																dl_2_src_on_tm

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1588	AFE_DL_SRC2_CON0_L	AFE_DL_SRC2 Control Register 0 Low Part	0000

																p_ctl_pre
Type																RW
Reset																0

Bit(s)	Name	Description
0	dl_2_src_on_tmp_ctl_pre	Turns on down-link

158A	AFE_UL_SRC_CON0_H	AFE Uplink SRC Control Register 0 High Part	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			c_digmic_phase_sel_ch1_ctl			c_digmic_phase_sel_ch2_ctl			c_two_digital_mic_ctl							
Type			RW			RW			RW							
Reset			0	0	0	0	0	0	0							

Bit(s)	Name	Description
13:11	c_digmic_phase_sel_ch1_ctl	**Selects 8 input phase latch**
10:8	c_digmic_phase_sel_ch2_ctl	**Selects 8 input phase latch**
7	c_two_digital_mic_ctl	**Turns on dual digital microphones mode** 0: Turn off 1: Turn on

158C	AFE_UL_SRC_CON0_L	AFE Uplink SRC Control Register 0 Low Part	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmic_low_power_mode_ctl										digmic_3p25m_1p625m_sel_ctl			ul_loop_back_mode_ctl	ul_sdm_3_level_ctl	ul_src_on_tmp_ctl
Type	RW										RW			RW	RW	RW
Reset	0	0									0			0	0	0

Bit(s)	Name	Description
15:14	dmic_low_power_mode_ctl	**Digital mic low power mode** 0: Original mode 1: 1.625m 48k mode 2: 812.5k low power mode 3: 406.25k low power mode

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Bit(s)	Name	Description
5	digmic_3p25m_1p625m_sel_ctl	**Digmic input mode 1** 0: 3.25M mode 1: 1.625M mode
2	ul_loop_back_mode_ctl	**Enables loopback mode from DL** 0: Normal UL 1: Loopback from DL
1	ul_sdm_3_level_ctl	**Selects SDM 3-level mode (digital MIC data path)** First priority choice. 0: De-select SDM 3-level mode 1: Select SDM 3-level mode
0	ul_src_on_tmp_ctl	**Turns on uplink SRC** 0: Turn off 1: Turn on

158E **AFE_TOP_CON0** **AFE Top Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ul_sine_on	dl_sine_on
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	ul_sine_on	**Enables UL sine table** 0: UL from up8x_rxif normal path 1: UL from sinetable
0	dl_sine_on	**Enables DL sine table** 0: DL from up8x_rxif normal path 1: DL from sinetable

1590 **AUDIO_TOP_CON0** **AUDIO Top Control Register 0** **C000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fifo_auto_rst_ctl	afe_ck_div_rst_ctl	pdn_adc_hires_ctl	afe_13m_phase_sel_ctl	afe_6p5m_phase_sel_ctl		afe_3p25m_phase_sel_ctl		pdn_afe_ctl	pdn_dac_ctl	pdn_adc_ctl	pdn_buckosc_ctl	pdn_i2s_dl_ctl	pwr_clk_dis_ctl	pdn_afe_testmodel_ctl	pdn_reserved
Type	RW	RW	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	fifo_auto_rst_ctl	**Reserved**
14	afe_ck_div_rst_ctl	**Digmic output clock (to analog) clock division circuit reset bit** 0: Not reset clock divider 1: Reset clock divider
13	pdn_adc_hires_ctl	**Powers down up-link hi-res**

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Bit(s)	Name	Description
		0: Not power down 1: Power down
12	afe_13m_phase_sel_ctl	**Reserved**
11:10	afe_6p5m_phase_sel_ctl	**Reserved**
9:8	afe_3p25m_phase_sel_ctl	**Reserved**
7	pdn_afe_ctl	**Powers down afe** 0: Not power down 1: Power down
6	pdn_dac_ctl	**Powers down down-link** 0: Not power down 1: Power down
5	pdn_adc_ctl	**Powers down up-link** 0: Not power down 1: Power down
4	pdn_buckosc_ctl	**Powers down buck osc clock** 0: Not power down 1: Power down
3	pdn_i2s_dl_ctl	**Reserved**
2	pwr_clk_dis_ctl	**Disables total audio clk** 0: Not power down 1: Power down
1	pdn_afe_testmodel_ctl	**Powers down some built-in test model clock source** 0: Not power down 1: Power down
0	pdn_reserved	0: Not power down 1: Power down

1592 **AFE_MON_DEBUG0** **AFE Monitor Output Debug Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	audio_sys_top_mon_swap			audio_sys_top_mon_sel					afe_mon_sel							
Type	RW			RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	audio_sys_top_mon_swap	**Swaps monitor output from 32 bits to 8 bits** 0: mon_out[7:0] 1: mon_out[15:8] 2: mon_out[23:16] 3: mon_out[31:24]
12:8	audio_sys_top_mon_sel	**Monitor output selection of audio system top level**
7:0	afe_mon_sel	**Monitor output selection of afe level**

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1594	AFUNC_AUD_CON0	A_FUNC AUDIO Control Register 0	D821

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cci_aud_anack_sel	cci_audio_fifo_wptr			cci_scrambler_cg_en	cci_lch_inv	cci_rand_en	cci_splt_scrmb_clk_on	cci_splt_scrmb_on	cci_aud_idac_test_en	cci_zero_pad_disable	cci_aud_split_test_en	cci_aud_sdm_mutel	cci_aud_sdm_muter	cci_aud_sdm_7bit_sel	cci_scrambler_en
Type	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	0	1	1	0	0	0	0	0	1	0	0	0	0	1

Bit(s)	Name	Description
15	cci_aud_anack_sel	**Analog 13m source inversion option** 0: Not invert AD_AUDDEC_13M_D5N_VCORE (or GPI) 1: Invert
14:12	cci_audio_fifo_wptr	**audio_fifo write pointer initial value**
11	cci_scrambler_cg_en	**Enables scrambler PA** 0: Disable scrambler PA 1: Enable scrambler PA
10	cci_lch_inv	**Selects sdm left channel out of phase** 0: In-phase with right channel 1: Out-of-phase with right channel
9	cci_rand_en	**Enables scrambler random** 0: Not random 1: Random
8	cci_splt_scrmb_clk_on	**Scrambler clock on** 0: Off 1: On
7	cci_splt_scrmb_on	**Enables scrambler output** 0: Off 1: On
6	cci_aud_idac_test_en	**Enables scrambler output test** 0: Normal path 1: From test_in
5	cci_zero_pad_disable	**Disables scrambler zero padding** 0: Zero-padding 1: Disable zero-padding
4	cci_aud_split_test_en	**Enables splitter test** 0: Normal path 1: From test_in ([12:8]/[7:4]/[2:0])
3	cci_aud_sdm_mutel	**Enables sdm output mute for left channel** Controlled by AFUNC_AUD_CON1[15:8]. 0: Not controlled by AFUNC_AUD_CON1 1: Controlled by AFUNC_AUD_CON1
2	cci_aud_sdm_muter	**Enables sdm output mute for left channel** Controlled by AFUNC_AUD_CON1[7:0]. 0: Not controlled by AFUNC_AUD_CON1 1: Controlled by AFUNC_AUD_CON1
1	cci_aud_sdm_7bit_sel	**Selects splitter** 0: From splitter1 1: From splitter3
0	cci_scrambler_en	**Enables scrambler** 0: Disable 1: Enable

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1596	AFUNC_AUD_CON1	A_FUNC AUDIO Control Register 1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aud_sdm_test_l								aud_sdm_test_r							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	aud_sdm_test_l	sdm mute test value for left channel
7:0	aud_sdm_test_r	sdm mute test value for right channel

1598	AFUNC_AUD_CON2	A_FUNC AUDIO Control Register 2	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									cci_aud_dac_ana_mute	cci_aud_dac_ana_rstb_sel		cci_audio_fifo_clkin_inv	cci_audio_fifo_enable	cci_acd_mode	cci_afifo_clk_pwdb	cci_acd_func_rstb
Type									RW	RW		RW	RW	RW	RW	RW
Reset									0	0		0	0	0	0	0

Bit(s)	Name	Description
7	cci_aud_dac_ana_mute	**Analog DAC interface mute (RG) control** 0: Analog DAC interface input from aud_dac_ana output (normal) 1: Analog DAC interface input from fixed mute patterns
6	cci_aud_dac_ana_rstb_sel	**Enables aud_dac_ana soft_rstb source selection** 0: aud_dac_ana reset by global rstb 1: aud_dac_ana reset by global rstb and cci_acd_func_rstb
4	cci_audio_fifo_clkin_inv	**Selects sdm 6.5M clock phase** 0: In-phase 1: Out-of-phase
3	cci_audio_fifo_enable	**Enables sdm audio_fifo** 0: Disable 1: Enable
2	cci_acd_mode	**sdm audio_fifo analog FT test mode** 0: Normal path 1: Test path from GPI, clock and data will be from GPI. For selection, see sdm_testck_src_sel.
1	cci_afifo_clk_pwdb	**sdm audio_fifo clock power down bit** 0: Power down 1: Power on
0	cci_acd_func_rstb	**sdm audio_fifo rstb bit** 0: Reset 1: Released

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159A	AFUNC_AUD_CON3	A_FUNC AUDIO Control Register 3	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sdm_ana13M_testck_sel	sdm_ana13M_testck_src_sel				sdm_testck_src_sel				digmic_testck_src_sel						digmic_testck_sel
Type	RW	RW				RW				RW						RW
Reset	0	0	0	0		0	0	0		0	0	0				0

Bit(s)	Name	Description
15	sdm_ana13M_testck_sel	**Selects sdm testck from GPI** 0: Normal path from digital output 1: Testing path from GPI. See the descriptions of sdm_ana13M_testck_src_sel in details.
14:12	sdm_ana13M_testck_src_sel	**Selects different GPI as sdm testck source** 0: test_ck_i[3] 1: test_ck_i[2] 2: test_ck_i[1] 3: test_ck_i[0] 4: test_in_i[0] 5: test_in_i[1] 6: test_in_i[3] 7: test_in_i[5]
10:8	sdm_testck_src_sel	**Selects different GPI as sdm testck source** 0: test_ck_i[3] 1: test_ck_i[2] 2: test_ck_i[1] 3: test_ck_i[0] 4: test_in_i[0] 5: test_in_i[1] 6: test_in_i[3] 7: test_in_i[5]
6:4	digmic_testck_src_sel	**Selects different GPI as digmic testck source** 0: test_ck_i[3] 1: test_ck_i[2] 2: test_ck_i[1] 3: test_ck_i[0] 4: test_in_i[2] 5: test_in_i[4] 6: test_in_i[6] 7: test_in_i[7]
0	digmic_testck_sel	**Selects digmic testck from GPI** 0: Normal path from digital output 1: Ttesting path from GPI. See the descriptions of digmic_testck_src_sel in details.

159C	AFUNC_AUD_CON4	A_FUNC AUDIO Control Register 4	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ul_fifo_wclk_inv		ul_fifo_digmic_w	ul_fifo_wdata_test	ul_fifo_wdata_test	ul_fifo_wclk_6p5	ul_fifo_wclk_6p5m_testck_src_sel		

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159C	AFUNC_AUD_CON4	A_FUNC AUDIO Control Register 4	0000

										data_test src_sel	en	src_sel	m_testck_sel			
Type								RW		RW	RW	RW	RW	RW		
Reset								0		0	0	0	0	0	0	0

Bit(s)	Name	Description
8	ul_fifo_wclk_inv	**Selects to invert ul fifo wclk** 0: Not invert 1: Invert ul fifo wclk.
6	ul_fifo_digmic_wdata_testsrc_sel	**Selects ul fifo digmic wdata from GPI (Test_in[1:0]) or tri-gen:** ch1: Test_in[1] ch2: Test_in[0] 0: Testing path from test input GPI, i.e. left channel ch1= test_in[1], right channel ch2 = test_in[0]. 1: Testing path from built-in tri-gen, ch1 uses tri_out[1], ch2 uses tri_out[0].
5	ul_fifo_wdata_testen	**Selects ul fifo wdata from others** 0: Normal path from analog output 1: Testing path from test input. See the descriptions of ul_fifo_wdata_testsrc_sel in details.
4	ul_fifo_wdata_testsrc_sel	**Enables GPI as ul fifo write testck source** 0: test input from GPI, i.e. left channel ch1[4:0]= test_in[4:0], right channel ch2[4:0] = test_in[4:0]. 1: Test input from tri-gen; both ch1 and ch2 use the same inputs from tri-gen.
3	ul_fifo_wclk_6p5m_testck_sel	**Enables GPI as ul fifo write testck source** 0: Normal path from analog 6p5M 1: From testck described in ul_fifo_wclk_6p5m_testck_src_sel
2:0	ul_fifo_wclk_6p5m_testck_src_sel	**Selects different GPI as ul fifo write testck source** 0: test_ck_i[2] 1: test_ck_i[2] 2: test_ck_i[1] 3: test_ck_i[0] 4: test_in_i[5] 5: test_in_i[6] 6: test_in_i[7] 7: test_in_i[0]

159E	AFUNC_AUD_MON0	A_FUNC AUDIO Monitor Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aud_scr_out_l								aud_scr_out_r							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	aud_scr_out_l	Scrambler/splitter debug output to read bus
7:0	aud_scr_out_r	Scrambler/splitter debug output to read bus

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15A0 **AUDRC_TUNE_MON0** **Analog Monitor Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	async_test_out_bck			RGS_AUDRCTUNE1READ								RGS_AUDRCTUNE0READ				
Type	RU			RU								RU				
Reset	0			0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
15	async_test_out_bck	
12:8	RGS_AUDRCTUNE1READ	AUDIOEN RC TUNE OUTPUT TO READ for 1 channel
4:0	RGS_AUDRCTUNE0READ	AUDIOEN RC TUNE OUTPUT TO READ for 0 channel

15BA **AFE_SGEN_CFG0** **AFE SGEN CON0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_amp_div_ch1_ctl								c_dac_en_ctl	c_mute_sw_ctl						
Type	RW								RW	RW						
Reset	0	0	0	0					0	0						

Bit(s)	Name	Description
15:12	c_amp_div_ch1_ctl	**Amplitude setting of channel 1 (SGEN)** 0: 0dB full scale 1: -6dB 2: -12dB 3: -18dB 4: -24dB 5: -30dB 6: -36dB 7: -42dB 8: -48dB 9: -54dB 10: -60dB 11: -66dB 12: -72dB 13: -78dB 14: -84dB 15: -90dB
7	c_dac_en_ctl	**Makes voice DAC output the test sine wave, signal generator (SGEN) configuration** 0: Disable sine waves output 1: Voice DAC inputs are sine waves
6	c_mute_sw_ctl	**Mute switch (SGEN)** 0: Turn on sine wave output in this test mode 1: Mute sine wave output

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15BC **AFE_SGEN_CFG1** **AFE SGEN CON1** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_sgen_rch_inv_5bit	c_sgen_rch_inv_8bit										c_freq_div_ch1_ctl				
Type	RW	RW										RW				
Reset	0	0										0	0	0	0	1

Bit(s)	Name	Description
15	c_sgen_rch_inv_5bit	**Inverts RCH sgen 5-bit data output**
14	c_sgen_rch_inv_8bit	**Inverts RCH sgen 8-bit data output**
4:0	c_freq_div_ch1_ctl	**Frequency setting of channel 1** 1X~15X for voice; 1X~31X for audio Frequency = Sampling rate/64*FREQ_DIV (SGEN) Sample rate: UL(8K/16K/32K -> 64K; 48K -> 96K); DL (8xFS)

15BE **AFE_ADC_ASYNC_FIFO_CFG** **AFE_ADC_SYNC_FIFO_CFG** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											rg_ul_async_fifo_soft_rst_en	rg_ul_async_fifo_soft_rst			rg_amic_ul_adc_clk_sel	
Type											RW	RW			RW	
Reset											0	1			0	

Bit(s)	Name	Description
5	rg_ul_async_fifo_soft_rst_en	**Selects UL async fifo soft reset** 0: UL async fifo use globle rst 1: UL async fifo use soft rst
4	rg_ul_async_fifo_soft_rst	**UL soft reset control** 0: UL fifo soft reset 1: Normal
1	rg_amic_ul_adc_clk_sel	**Selects ADC 0/1 channel latch clk** 0: Select ana_ch0 ck 1: Select ana_ch1 ck

15C0 **AFE_DCCLK_CFG0** **AFE_DCCLK_CFG0** **0FE2**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dcclk_div											dcclk	dcclk_ref_		dcclk	dcclk

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15C0 **AFE_DCCLK_CFG0** **AFE_DCCLK_CFG0** **0FE2**

												_inv	ck_sel		_pd n	_gen _on
Type	RW											RW	RW		RW	RW
Reset	0	0	0	0	1	1	1	1	1	1	1	0	0	0	1	0

Bit(s)	Name	Description
15:5	dcclk_div	**dcclk divider** dcclk = 13M(12.854M)/(div+1)
4	dcclk_inv	**dcclk inverter**
3:2	dcclk_ref_ck_sel	**Selects dcclk reference clock** 00: Normal 26M/2 01: Vow 12.854M 10: buck_oscclk 11: buck_oscclk
1	dcclk_pdn	**dcclk power down control** 0: dcclk output 1: Power down dcclk
0	dcclk_gen_on	**Enables dcclk generation** 0: Disable 1: Enable

15C2 **AFE_DCCLK_CFG1** **AFE_DCCLK_CFG1** **1105**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				da_audvowclk_buckosc_pdn	resync_src_sel		resync_src_ck_inv	dcclk_resync_bypass	dcclk_phase_sel				da_audvowclk_buckosc_div			
Type				RW	RW		RW	RW	RW				RW			
Reset				1	0	0	0	1	0	0	0	0	0	1	0	1

Bit(s)	Name	Description
12	da_audvowclk_buckosc_pdn	**Powers down da_audvowclk_buckosc** 0: Enable 1: Power down
11:10	resync_src_sel	**Selects dcclk resync clock** 00: adcsync_clk 01: Vow 12.854M 10: buck_oscclk 11: 26m clock
9	resync_src_ck_inv	**dcclk resync clock inverter**
8	dcclk_resync_bypass	**dcclk bypass resync** 0: resync 1: Bypass resync
7:4	dcclk_phase_sel	**Selects dcclk resync phase**
3:0	da_audvowclk_buckosc_div	**da_audvowclk_buckosc divider**

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1606	AUDENC_ANA_CON0	AUDENC Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_AUDADCLINPUTSEL		RG_AUDADCLPWRUP		RG_AUDPREAMPLGAIN			RG_AUDPREAMPLINPUTSEL		RG_AUDPREAMPLVSCALE		RG_AUDPREAMPLPGATEST	RG_AUDPREAMPLDCRPECHARGE	RG_AUDPREAMPLDCCEN	RG_AUDPREAMPLON
Type		RW		RW		RW			RW		RW		RW	RW	RW	RW
Reset		0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:13	RG_AUDADCLINPUTSEL	**Selects audio L ADC input** 00: Idle 01: AIN0 10: Left preamplifier 11: Idle
12	RG_AUDADCLPWRUP	**Powers up audio L ADC** 0: Power down 1: Power on
10:8	RG_AUDPREAMPLGAIN	**Adjusts audio L preamplifier gain** 000: 0dB 001: 6dB 010: 12dB 011: 18dB 100: 24dB
7:6	RG_AUDPREAMPLINPUTSEL	**Selects audio L preamplifier input** 00: None 01: AIN0 10: AIN1 11: AIN2
5:4	RG_AUDPREAMPLVSCALE	**Audio L preamplifier PGA DC output voltage scale**
3	RG_AUDPREAMPLPGATEST	**Enables audio L preamplifier PGA test** 0: Disable 1: Enable
2	RG_AUDPREAMPLDCRPECHARGE	**Audio L preamplifier PGA DC couple input precharge** 0: Disable 1: Enable
1	RG_AUDPREAMPLDCCEN	**Audio L DC couple input** 0: AC couple input 1: DC couple input
0	RG_AUDPREAMPLON	**Enables audio L preamplifier** 0: Disable 1: Enable

1608	AUDENC_ANA_CON1	AUDENC Control Register 1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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1608 **AUDENC_ANA_CON1** **AUDENC Control Register 1** **0000**

Name		**RG_AUDADCRINPUTSEL**		**RG_AUDADCRPWRUP**		**RG_AUDPREAMPRGAIN**			**RG_AUDPREAMPRINPUTSEL**		**RG_AUDPREAMPRVSCALE**		**RG_AUDPREAMPRPGATEST**	**RG_AUDPREAMPRDCRPECHARGE**	**RG_AUDPREAMPRDCCEN**	**RG_AUDPREAMPRON**
Type		RW		RW		RW			RW		RW		RW	RW	RW	RW
Reset		0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:13	RG_AUDADCRINPUTSEL	**Selects audio R ADC input** 00: Idle 01: AIN0 10: Right preamplifier 11: Idle
12	RG_AUDADCRPWRUP	**Powers up audio R ADC** 0: Power down 1: Power on
10:8	RG_AUDPREAMPRGAIN	**Adjusts audio R preamplifier gain** 000: 0dB 001: 6dB 010: 12dB 011: 18dB 100: 24dB
7:6	RG_AUDPREAMPRINPUTSEL	**Selects audio R preamplifier input** 00: None 01: AIN0 10: AIN1 11: AIN2
5:4	RG_AUDPREAMPRVSCALE	**Audio R preamplifier PGA DC output voltage scale**
3	RG_AUDPREAMPRPGATEST	**Enables audio R preamplifier PGA test** 0: Disable 1: Enable
2	RG_AUDPREAMPRDCRPECHARGE	**Audio R preamplifier PGA DC couple input precharge** 0: Disable 1: Enable
1	RG_AUDPREAMPRDCCEN	**Audio R DC couple input** 0: AC couple input 1: DC couple input
0	RG_AUDPREAMPRON	**Enables audio R preamplifier** 0: Disable 1: Enable

160A **AUDENC_ANA_CON2** **AUDENC Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_AUDADCFLASHIDDTEST**		**RG_AUDADCREFBUFIDDTEST**		**RG_AUDADC2NDSTAGEIDDTES**		**RG_AUDADC1STSTAGEIDDTES**		**RG_AUDPREAMPIDDTEST**		**RG_AUDADC**	**RG_AUDADC**	**RG_AUDADC**	**RG_AUDPRE**	**RG_AUDGLB**	**RG_AUDULH**

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160A	AUDENC_ANA_CON2	AUDENC Control Register 2	0000

					T		T				FLASHLPEN	2NDSTAGELPEN	1STSTAGELPEN	AMPLPEN	MADLPWEN	ALFBIAS
Type	RW		RW		RW		RW		RW		RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	RG_AUDADCFLASHIDDTEST	**Selects audio ADC flash Idd current test selection** 00: 100% 01: 80% 10: 120% 11: 140%
13:12	RG_AUDADCREFBUFIDDTEST	**Selects audio ADC reference buffer Idd current test** 00: 100% 01: 80% 10: 120% 11: 140%
11:10	RG_AUDADC2NDSTAGEIDDTEST	**Audio ADC 2nd & 3rd stage Idd adjust bits** 00: 100% 01: 80% 10: 120% 11: 140%
9:8	RG_AUDADC1STSTAGEIDDTEST	**Audio ADC 1st stage Idd adjust bits** 00: 100% 01: 80% 10: 120% 11: 140%
7:6	RG_AUDPREAMPIDDTEST	**Audio preamplifier Idd adjust bits** 00: 100% 01: 75% 10: 125% 11: 150%
5	RG_AUDADCFLASHLPEN	**Enables audio ADC flash low power** 0: Normal 1: Enable
4	RG_AUDADC2NDSTAGELPEN	**Enables audio ADC 2nd & 3rd low power** 0: Normal 1: Enable
3	RG_AUDADC1STSTAGELPEN	**Enables audio ADC 1st Stage low power** 0: Normal 1: Enable
2	RG_AUDPREAMPLPEN	**Audio preamplifier PGA low power mode** 0: Disable 1: Enable
1	RG_AUDGLBMADLPWEN	**Enables audio uplink globe bias VOW low power mode** 0: Normal 1: Enable
0	RG_AUDULHALFBIAS	**Enables audio uplink halfbias** 0: Normal 1: Enable

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160C	AUDENC_ANA_CON3	AUDENC Control Register 3	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDSPAREPGA	RG_DCCVCMBUFLPSWEN	RG_DCCVCMBUFLPMODSEL	RG_AUDPREAMPAAFEN					RG_AUDADCCLKSOURCE		RG_AUDADCCLKSEL	RG_AUDADCDAC0P25FS
Type					RW	RW	RW	RW					RW		RW	RW
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11	RG_AUDSPAREPGA	**Spare control bits for PGA**
10	RG_DCCVCMBUFLPSWEN	**Audio preamplifier PGA DCC VCM buffer SW EN**
9	RG_DCCVCMBUFLPMODSEL	**Audio preamplifier PGA DCC VCM buffer LP MODSEL**
8	RG_AUDPREAMPAAFEN	**Audio preamplifier PGA with AAF input in DC couple mode** 0: Disable 1: Enable
3:2	RG_AUDADCCLKSOURCE	**Audio ADC clock source** 00: 26MHz from CLKSQ 01: 26MHz from CLKSQ test 10: 12.58MHz from 32kHz PLL 11: None
1	RG_AUDADCCLKSEL	**Selects audio ADC clock** 0: 6.5MHz clock in, 3.25MHz data out 1: 13MHz clock in, 6.5MHz data out
0	RG_AUDADCDAC0P25FS	**Enables audio ADC FBDAC 0.25FS** 0: 6.5MHz clock in, 3.25MHz data out 1: 3.25MHz clock in, 1.625MHz data out

160E	AUDENC_ANA_CON4	AUDENC Control Register 4	0800

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDADCDACTEST	RG_AUDADCNODEM	RG_AUDADCDACNRZ	RG_AUDADCDACIDDTEST		RG_AUDADCDACFBCURRENT	RG_AUDADCFFBYPASS	RG_AUDADCBYPASS	RG_AUDADCNOPATEST	RG_AUDADCWIDECM	RG_AUDADCFSRESET	RG_AUDADC3RDSTAGERESET	RG_AUDADC2NDSTAGERESET	RG_AUDADC1STSTAGESDENB
Type			RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	RG_AUDADCDACTEST	**Audio ADC DAC test** 0: Disable 1: Enable data in RG_AUDADCTESTDATA[15:0] to be passed to the DAC
12	RG_AUDADCNODE	**Audio ADC DEM test**

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Bit(s)	Name	Description
	M	
11	RG_AUDADCDACNRZ	**Audio ADC DAC in non return to zero mode** 0: RZ mode (2I) 1: NRZ mod (I)
10:9	RG_AUDADCDACIDDTEST	**Selects audio ADC-DAC Idd current test** 00: Normal 11: -20% DAC f/b current
8	RG_AUDADCDACFBCURRENT	**Audio ADC feedback coefficient**
7	RG_AUDADCFFBYPASS	**Audio ADC feed forward bypass** 0: No bypass. Allow feedforward coefficient to pass signal to ADC flash. 1: Bypass. Not allow ADC i/p signal to feedforward flash.
6	RG_AUDADCBYPASS	**Enables audio ADC input resistor bypass** 0: Disable 1: Enable
5	RG_AUDADCNOPATEST	**Audio ADC no preamp test** 0: Normal ADC gain 1: 6dB ADC gain
4	RG_AUDADCWIDECM	**Enables audio ADC wide common mode** 0: Normal 1: Enable
3	RG_AUDADCFSRESET	**Selects audio encoder FS reset block model**
2	RG_AUDADC3RDSTAGERESET	**Resets audio ADC 3rd stage** 0: Normal 1: Reset
1	RG_AUDADC2NDSTAGERESET	**Resets audio ADC 2nd stage** 0: Normal 1: Reset
0	RG_AUDADC1STSTAGESDENB	**Audio ADC 1st stage source degenerate enableb** 0: Enable 1: Disable

1610 **AUDENC_ANA_CON5** **AUDENC Control Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDADCTESTDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_AUDADCTESTDATA	**Audio ADC test data bits** Audio ADC test data bits for both phases of DRTZ DAC. Can enable any current source you select.

1612 **AUDENC_ANA_CON6** **AUDENC Control Register 6** **1515**

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1612	AUDENC_ANA_CON6	AUDENC Control Register 6	1515

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDRCTUNERSEL	RG_AUDRCTUNER							RG_AUDRCTUNELSEL	RG_AUDRCTUNEL				
Type			RW	RW							RW	RW				
Reset			0	1	0	1	0	1			0	1	0	1	0	1

Bit(s)	Name	Description
13	RG_AUDRCTUNERSEL	**Selects audio R ADC RC tuning** 0: Use auto cal tune bits 1: Use RG_AUDRCTUNEL[4:0]
12:8	RG_AUDRCTUNER	**Audio R ADC RC tuned value** See RG_AUDRCTUNELSE.
5	RG_AUDRCTUNELSEL	**Selects audio L ADC RC tuning** 0: Use auto cal tune bits 1: Use RG_AUDRCTUNEL[4:0]
4:0	RG_AUDRCTUNEL	**Audio L ADC RC tuned value** See RG_AUDRCTUNELSE.

1614	AUDENC_ANA_CON7	AUDENC Control Register 7	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDENCSPAREVA18				RG_AUDENCSPAREVA28				RG_AUDSPAREVA18				RG_AUDSPAREVA28			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	RG_AUDENCSPAREVA18	Spare control bits for AVDD12 voltage domain
11:8	RG_AUDENCSPAREVA28	Spare control bits for AVDD25 voltage domain
7:4	RG_AUDSPAREVA18	Spare control bits for AVDD12 voltage domain
3:0	RG_AUDSPAREVA28	Spare control bits for AVDD25 voltage domain

1616	AUDENC_ANA_CON8	AUDENC Control Register 8	0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDSPAREVMIC				RG_DMICMONSEL			RG_DMICMONEN	RG_AUDDIGMICNDUTY		RG_AUDDIGMICPDUTY		RG_DMICHPCLKEN	RG_AUDDIGMICBIAS		RG_AUDDIGMICEN
Type	RW				RW			RW	RW		RW		RW	RW		RW

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1616	AUDENC_ANA_CON8	AUDENC Control Register 8	0004

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15:12	RG_AUDSPAREVMIC	**Spare control bits for AVDD25MIC voltage domain**
11:9	RG_DMICMONSEL	**Digital microphone monitor path**
8	RG_DMICMONEN	**Enables digital microphone monitor path** 0: Disable 1: Enable
7:6	RG_AUDDIGMICNDUTY	**Digital microphone negative duty control**
5:4	RG_AUDDIGMICPDUTY	**Digital microphone positive duty control**
3	RG_DMICHPCLKEN	**Digital microphone CLK source from** 0: Digital 1: CLKSQ
2:1	RG_AUDDIGMICBIAS	**Digital microphone slew rate control** 11 > 10 > 01 > 00
0	RG_AUDDIGMICEN	**Enables digital microphone** 0: Disable 1: Enable

1618	AUDENC_ANA_CON9	AUDENC Control Register 9	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_AUDMICBIAS0DCSW2NEN	RG_AUDMICBIAS0DCSW2P2EN	RG_AUDMICBIAS0DCSW2P1EN		RG_AUDMICBIAS0DCSW0NEN	RG_AUDMICBIAS0DCSW0P2EN	RG_AUDMICBIAS0DCSW0P1EN		RG_AUDMICBIAS0VREF				RG_AUDMICBIAS0LOWPEN	RG_AUDMICBIAS0BYPASSEN	RG_AUDPWDBMICBIAS0
Type		RW	RW	RW		RW	RW	RW		RW				RW	RW	RW
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
14	RG_AUDMICBIAS0DCSW2NEN	**MIC Bias 0 DC couple switch 2N** 0: Off 1: On
13	RG_AUDMICBIAS0DCSW2P2EN	**MIC Bias 0 DC couple switch 2P2** 0: Off 1: On
12	RG_AUDMICBIAS0DCSW2P1EN	**MIC Bias 0 DC couple switch 2P1** 0: Off 1: On
10	RG_AUDMICBIAS0DCSW0NEN	**MIC Bias 0 DC couple switch 0N** 0: Off 1: On

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Bit(s)	Name	Description
9	RG_AUDMICBIAS0DCSW0P2EN	**MIC Bias 0 DC couple switch 0P2** 0: Off 1: On
8	RG_AUDMICBIAS0DCSW0P1EN	**MIC Bias 0 DC couple switch 0P1** 0: Off 1: On
6:4	RG_AUDMICBIAS0VREF	**Selects MIC Bias 0 output voltage** 000: 1.7V 001: 1.8V 010: 1.9V 011: 2.0V 100: 2.1V 101: 2.5V 110: Test 2.6V 111: Test 2.7V
2	RG_AUDMICBIAS0LOWPEN	**Enables MIC Bias 0 LowPower** 0: Normal mode 1: Low power mode
1	RG_AUDMICBIAS0BYPASSEN	**Enables MIC Bias 0 BYPASS 2P8V** 1: enable 0: Disable 1: Enable
0	RG_AUDPWDBMICBIAS0	**Powers down MIC Bias 0** 0: Power down 1: Power on

161A **AUDENC_ANA_CON10** **AUDENC Control Register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RG_BANDGAPGEN**			**RG_AUDMICBIAS1DCSW1NEN**	**RG_AUDMICBIAS1DCSW1PEN**		**RG_AUDMICBIAS1VREF**				**RG_AUDMICBIAS1LOWPEN**	**RG_AUDMICBIAS1BYPASSEN**	**RG_AUDPWDBMICBIAS1**
Type				RW			RW	RW		RW				RW	RW	RW
Reset				0			0	0		0	0	0		0	0	0

Bit(s)	Name	Description
12	RG_BANDGAPGEN	**Remote sense to bandgap ground** 0: Disable 1: Enable
9	RG_AUDMICBIAS1DCSW1NEN	**MIC Bias 1 DC couple switch 1N** 0: Off 1: On
8	RG_AUDMICBIAS1DCSW1PEN	**MIC Bias 1 DC couple switch 1P** 0: Off 1: On
6:4	RG_AUDMICBIAS1VREF	**Selects MIC Bias 1 output voltage** 000: 1.7V 001: 1.8V 010: 1.9V

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Bit(s)	Name	Description
		011: 2.0V 100: 2.1V 101: 2.5V 110: Test 2.6V 111: Test 2.7V
2	RG_AUDMICBIAS1LOWPEN	**Enables MIC Bias 1 LowPower** 0: Normal mode 1: Low power mode
1	RG_AUDMICBIAS1BYPASSEN	**Enables MIC Bias 1 BYPASS 2P8V** 0: Disable 1: Enable
0	RG_AUDPWDBMICBIAS1	**Powers down MIC Bias 1** 0: Power down 1: Power on

161C **AUDENC_ANA_CON11** **AUDENC Control Register 11** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ACCDETSPAREVA28			RG_EINTHIRENB	RG_EINTCONFIGACCDET	RG_EINTCOMPVTH	RG_SWBUFSWEN	RG_SWBUFMODSEL	RG_ACCDETSEL	RG_AUDACCDETTVDET	RG_AUDACCDETVTHBCAL	RG_AUDACCDETVTHACAL		RG_AUDACCDETVIN1PULLLOW	RG_AUDACCDETMICBIAS1PULLLOW	RG_AUDACCDETMICBIAS0PULLLOW
Type	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
15:13	RG_ACCDETSPAREVA28	**Spare control bits for ACCDET**
12	RG_EINTHIRENB	**Selects EINT High R** 0: 2M 1: 500k
11	RG_EINTCONFIGACCDET	**Internal connection between ACCDET and EINT** 0: Disable 1: Enable (EINT connected with ACCDET pin; ACCDETSEL should be 1)
10	RG_EINTCOMPVTH	**EINT comparator threshold** 0: 6/8 => 2.4V 1: 5/8 => 2V
9	RG_SWBUFSWEN	**Switch buffer turn on SW mode control for ACCDET to AUXADC** 0: Power down 1: Power on
8	RG_SWBUFMODSEL	**Buffer power control** 0: Hardware mode 1: Software mode
7	RG_ACCDETSEL	**Selects ACCDET input** 0: ACCDET pin 1: MICP pin
6	RG_AUDACCDETT	**Puts audio accessory detection into TV mode**

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Bit(s)	Name	Description
	VDET	0: Disable 1: Enable
5	RG_AUDACCDETVTHBCAL	**Audio accessory detection voltage threshold B calibration**
4	RG_AUDACCDETVTHACAL	**Audio accessory detection voltage threshold A calibration**
2	RG_AUDACCDETVIN1PULLLOW	**Pulls low VIN1 pads when MICBIAS is off** 0: Disable 1: Enable
1	RG_AUDACCDETMICBIAS1PULLLOW	**Pulls low MIC Bias 1 pads when MICBIAS is off** 0: Disable 1: Enable
0	RG_AUDACCDETMICBIAS0PULLLOW	**Pulls low MIC Bias 0 pads when MICBIAS is off** 0: Disable 1: Enable

161E **AUDENC_ANA_CON12** **AUDENC Control Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RGS_AUDRCTUNERREAD								RGS_AUDRCTUNELREAD				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
12:8	RGS_AUDRCTUNERREAD	**Audio R RC tune read data**
4:0	RGS_AUDRCTUNELREAD	**Audio L RC tune read data**

1646 **AUDDEC_ANA_CON0** **AUDDEC Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDHPRBSCCURRENT_VAUDP15	RG_AUDHPLBSCCURRENT_VAUDP15	RG_AUDHPRSCDISABLE_VAUDP15	RG_AUDHPLSCDISABLE_VAUDP15	RG_AUDHPRMUXINPUTSEL_VAUDP15		RG_AUDHPLMUXINPUTSEL_VAUDP15		RG_AUDHPRPWRUP_IBIAS_VAUDP15	RG_AUDHPLPWRUP_IBIAS_VAUDP15	RG_AUDHPRPWRUP_VAUDP15	RG_AUDHPLPWRUP_VAUDP15	RG_AUD_DAC_PWL_UP_VA28	RG_AUD_DAC_PWR_UP_VA28	RG_AUDDACRPWRUP_VAUDP15	RG_AUDDACLPWRUP_VAUDP15
Type	RW	RW	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_AUDHPRBSCCURRENT_VAUDP15	**Audio right headphone BSC current**
14	RG_AUDHPLBSCCURRENT_VAUDP15	**Audio left headphone BSC current**

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Bit(s)	Name	Description
13	RG_AUDHPRSCDISABLE_VAUDP15	**Disables headphone right short circuit protection**
12	RG_AUDHPLSCDISABLE_VAUDP15	**Disables headphone left short circuit protection**
11:10	RG_AUDHPRMUXINPUTSEL_VAUDP15	**Selects audio right headphone input multiplexor** Positive/negative pins: 00: Open/Open 01: LOLP/LOLN 10: IDACRP/IDACRN 11 HSP/HSN (test mode)
9:8	RG_AUDHPLMUXINPUTSEL_VAUDP15	**Selects audio left headphone input multiplexor Positive/negative pins:** 00: Open/Open 01: LOLP/LOLN 10: IDACRP/IDACRN 11 HSP/HSN (test mode)
7	RG_AUDHPRPWRUP_IBIAS_VAUDP15	**Powers up audio right headphone bias**
6	RG_AUDHPLPWRUP_IBIAS_VAUDP15	**Powers up audio left headphone bias**
5	RG_AUDHPRPWRUP_VAUDP15	**Powers up audio right headphone**
4	RG_AUDHPLPWRUP_VAUDP15	**Powers up audio left headphone**
3	RG_AUD_DAC_PWL_UP_VA28	**Power down control for left channel audio biasgen** 0: Power down 1: Enable
2	RG_AUD_DAC_PWR_UP_VA28	**Power down control for right channel audio biasgen** 0: Power down 1: Enable
1	RG_AUDDACRPWRUP_VAUDP15	**Power down control for right-channel audio DAC** 0: Power down 1: Enable
0	RG_AUDDACLPWRUP_VAUDP15	**Power down control for left-channel audio DAC** 0: Power down 1: Enable

1648 **AUDDEC_ANA_CON1** **AUDDEC Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**RG_HPROUTSTGCTRL_VAUDP15**			**RG_HPLOUTSTGCTRL_VAUDP15**			**RG_HPRSHORT2HPRAUX_EN_VAUDP15**	**RG_HPLSHORT2HPLAUX_EN_VAUDP15**	**RG_HPRAUXFBRSW_EN_VAUDP15**	**RG_HPLAUXFBRSW_EN_VAUDP15**	**RG_AUDHPROUTAUXPWRUP_VAUDP15**	**RG_AUDHPLOUTAUXPWRUP_VAUDP15**	**RG_AUDHPROUTPWRUP_VAUDP15**	**RG_AUDHPLOUTPWRUP_VAUDP15**
Type			RW			RW			RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
13:11	RG_HPROUTSTGCTRL_VAUDP15	**Selects audio right headphone output stage** 000: 1x 001: 2x 010: 3x 011: 4x 100: 5x 101: 6x 110: 7x 111: 8x
10:8	RG_HPLOUTSTGCTRL_VAUDP15	**Selects audio left headphone output stage** 000: 1x 001: 2x 010: 3x 011: 4x 100: 5x 101: 6x 110: 7x 111: 8x
7	RG_HPRSHORT2HPRAUX_EN_VAUDP15	**Enables audio right headphone main and aux output stages short**
6	RG_HPLSHORT2HPLAUX_EN_VAUDP15	**Enables audio left headphone main and aux output stages short**
5	RG_HPRAUXFBRSW_EN_VAUDP15	**Enables audio right headphone aux feedback resistor for audio depop**
4	RG_HPLAUXFBRSW_EN_VAUDP15	**Enables audio left headphone aux feedback resistor**
3	RG_AUDHPROUTAUXPWRUP_VAUDP15	**Powers up audio right headphone aux output stage**
2	RG_AUDHPLOUTAUXPWRUP_VAUDP15	**Powers up audio left headphone aux output stage**
1	RG_AUDHPROUTPWRUP_VAUDP15	**Powers up audio right headphone main output stage**
0	RG_AUDHPLOUTPWRUP_VAUDP15	**Powers up audio left headphone main output stage**

164A **AUDDEC_ANA_CON2** **AUDDEC Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_HPPSHORT2VCM_VAUDP15	RG_AUDREFN_DERES_EN_VAUDP15	RG_AUDHPSTARTUP_VAUDP15							RG_HPROUTPUTSTBENH_VAUDP15				RG_HPLOUTPUTSTBENH_VAUDP15		
Type	RW	RW	RW							RW				RW		
Reset	0	0	0							0	0	0		0	0	0

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Bit(s)	Name	Description
15	RG_HPPSHORT2VCM_VAUDP15	**HP driver positive output stage short to AU_REFN**
14	RG_AUDREFN_DERES_EN_VAUDP15	**Enables HP ESD resistor @AU_REFN short**
13	RG_AUDHPSTARTUP_VAUDP15	**Forces startup mode in HP Amps if required**
6:4	RG_HPROUTPUTSTBENH_VAUDP15	**Enhances HPR output stage STB** 000: Open 001: 240 010: 490 011: 1k 100: 2k 101: 4k 110~111: Unused
2:0	RG_HPLOUTPUTSTBENH_VAUDP15	**Enhances HPL output stage STB** 000: Open 001: 240 010: 490 011: 1k 100: 2k 101: 4k 110~111: Unused

164C **AUDDEC_ANA_CON3** **AUDDEC Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_HPOUTPUTRESET0_VAUDP15	RG_HPINPUTRESET0_VAUDP15	RG_HPINPUTSTBENH_VAUDP15													
Type	RW	RW	RW													
Reset	0	0	0													

Bit(s)	Name	Description
15	RG_HPOUTPUTRESET0_VAUDP15	**HPL/R driver SE output reset to 0V ground** 0: No reset 1: Reset
14	RG_HPINPUTRESET0_VAUDP15	**HP driver input reset to ground** 0: No reset 1: Reset
13	RG_HPINPUTSTBENH_VAUDP15	**HP driver input stability enhancement option** 0: No enhancement 1: Enhance

164E **AUDDEC_ANA_CON4** **AUDDEC Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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164E **AUDDEC_ANA_CON4** **AUDDEC Control Register 4** **0000**

Name	**RG_AUDHPCOMP_EN_VAUDP15**		**RG_AUDHPHFCOMPBUFGAINSEL_VAUDP15**			**RG_AUDHPHFCOMPRESSEL_VAUDP15**				**RG_AUDHPLFCOMPRESSEL_VAUDP15**				**RG_AUDHPDIFFINPBIASADJ_VAUDP15**		
Type	RW		RW			RW				RW				RW		
Reset	0		0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
15	RG_AUDHPCOMP_EN_VAUDP15	**Enables HP driver core compensation circuit (unused)**
13:12	RG_AUDHPHFCOMPBUFGAINSEL_VAUDP15	**Selects HP driver core HF compensation buffer gain** 00~11: Unused
10:8	RG_AUDHPHFCOMPRESSEL_VAUDP15	**Selects HP driver core HF compensation resistor** 000: 1x 001: 2x 010: 4x 011: 6x 100: 8x 101: 10x 110: 12x 111: 14x (unused)
6:4	RG_AUDHPLFCOMPRESSEL_VAUDP15	**Selects HP driver core LF compensation resistor** 000: 1x 001: 2x 010: 4x 011: 6x 100: 8x 101: 10x 110: 12x 111: 14x (unused)
2:0	RG_AUDHPDIFFINPBIASADJ_VAUDP15	**Selects HP driver input differential pair bias current** 000: 20u 001: 40u 010: 80u 011: 160u 100: 240u 101: 280u 110: 320u 111: 360u (unused)

1650 **AUDDEC_ANA_CON5** **AUDDEC Control Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**RG_AUDHPDEDMGAINADJ_VAUDP15**				**RG_AUDHPDECMGAINADJ_VAUDP15**		
Type										RW				RW		
Reset										0	0	0		0	0	0

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Bit(s)	Name	Description
6:4	RG_AUDHPDEDMGAINADJ_VAUDP15	**HP driver differential mode gain degeneration** 000: 1x 001: 0.5x 010: 0.25x 011: 0.1x 100: 0.05x 101~111: Unused
2:0	RG_AUDHPDECMGAINADJ_VAUDP15	**HP driver common mode gain degeneration** 000: 1x 001: 0.5x 010: 0.25x 011: 0.1x 100: 0.05x 101~111: Unused

1652 **AUDDEC_ANA_CON6** **AUDDEC Control Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_HSOUT_SHORTVCM_VAUDP15	RG_HSOUTPUTRESET0_VAUDP15	RG_HSINPUTRESET0_VAUDP15	RG_HSINPUTSTBENH_VAUDP15	RG_HSOUTPUTSTBENH_VAUDP15	RG_AUDHSSTARTUP_VAUDP15	RG_AUDHSBSCCURRENT_VAUDP15	RG_AUDHSSCDISABLE_VAUDP15	RG_AUDHSMUXINPUTSEL_VAUDP15		RG_AUDHSPWRUP_IBIAS_VAUDP15	RG_AUDHSPWRUP_VAUDP15
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	RG_HSOUT_SHORTVCM_VAUDP15	**Short HS output to VCM (DCC: 0V; ACC: 1.4V)** 0: Not short to VCM 1: Short to VCM
10	RG_HSOUTPUTRESET0_VAUDP15	**HS driver DE outputs reset to 0V ground** 0: No reset 1: Reset
9	RG_HSINPUTRESET0_VAUDP15	**HS driver DE inputs reset to 0V ground** 0: No reset 1: Reset
8	RG_HSINPUTSTBENH_VAUDP15	**HS driver input stability enhancement option** 0: No enhancement 1: Enhance
7	RG_HSOUTPUTSTBENH_VAUDP15	**HS driver output stability enhancement option** 0: No enhancement 1: Enhance
6	RG_AUDHSSTARTUP_VAUDP15	**Forces startup mode in HS Amp if required**
5	RG_AUDHSBSCCURRENT_VAUDP15	**Audio handset BSC current**
4	RG_AUDHSSCDISABLE_VAUDP15	**Disables headset short circuit protection**
3:2	RG_AUDHSMUXIN	**Selects audio handset input multiplexor**

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Bit(s)	Name	Description
	PUTSEL_VAUDP15	Positive/negative pins: 00: Open/Open 01: MUTE (input grounded) 10: Voice playback 11: Test mode
1	RG_AUDHSPWRUP_IBIAS_VAUDP15	**Powers up audio headset bias**
0	RG_AUDHSPWRUP_VAUDP15	**Powers up audio headset**

1654 **AUDDEC_ANA_CON7** **AUDDEC Control Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RG_LOOUT_SHORTVCM_VAUDP15**	**RG_LOOUTPUTRESETo_VAUDP15**	**RG_LOINPUTRESETo_VAUDP15**	**RG_LOOUTPUTSTBENH_VAUDP15**	**RG_LOINPUTSTBENH_VAUDP15**	**RG_AUDLOSTARTUP_VAUDP15**	**RG_AUDLOLBSCCURRENT_VAUDP15**	**RG_AUDLOLSCDISABLE_VAUDP15**	**RG_AUDLOLMUXINPUTSEL_VAUDP15**		**RG_AUDLOLPWRUP_IBIAS_VAUDP15**	**RG_AUDLOLPWRUP_VAUDP15**
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	RG_LOOUT_SHORTVCM_VAUDP15	0: Not short to VCM 1: Short to VCM
10	RG_LOOUTPUTRESETo_VAUDP15	**LOL/R driver SE output reset to 0V ground** 0: No reset 1: Reset
9	RG_LOINPUTRESETo_VAUDP15	**LO driver input reset to ground** 0: No reset 1: Reset
8	RG_LOOUTPUTSTBENH_VAUDP15	**LO driver output stability enhancement option** 0: No enhancement 1: Enhance
7	RG_LOINPUTSTBENH_VAUDP15	**LO driver input stability enhancement option** 0: No enhancement 1: Enhance
6	RG_AUDLOSTARTUP_VAUDP15	**Forces startup mode in LO Amps if required**
5	RG_AUDLOLBSCCURRENT_VAUDP15	**Audio left LO buffer BSC current**
4	RG_AUDLOLSCDISABLE_VAUDP15	**Disables LO buffer left short circuit protection**
3:2	RG_AUDLOLMUXINPUTSEL_VAUDP15	**Selects audio left LO buffer input multiplexor** Positive/negative pins: 00: Open/open 01: MUTE (input grounded) 10: Audio playback 11: Test mode
1	RG_AUDLOLPWRU	**Powers up audio left LO buffer bias**

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Bit(s)	Name	Description
	P_IBIAS_VAUDP15	
0	RG_AUDLOLPWRUP_VAUDP15	**Powers up audio left LO buffer**

1656 **AUDDEC_ANA_CON8** **AUDDEC Control Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RG_AUDHPSPKDET_EN_VAUDP15**	**RG_AUDHPSPKDET_OUTPUTMUXSEL_VAUDP15**		**RG_AUDHPSPKDET_INPUTMUXSEL_VAUDP15**			**RG_AUDTRIMBUF_EN_VAUDP15**	**RG_AUDTRIMBUF_GAINSEL_VAUDP15**		**RG_AUDTRIMBUF_INPUTMUXSEL_VAUDP15**			
Type				RW	RW		RW			RW	RW		RW			
Reset				0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
12	RG_AUDHPSPKDET_EN_VAUDP15	**Enables audio headphone speaker detection**
11:10	RG_AUDHPSPKDET_OUTPUTMUXSEL_VAUDP15	**Selects audio headphone speaker detection output mux** 00: Open 01: HPL 10: HPR 11: Unused
9:8	RG_AUDHPSPKDET_INPUTMUXSEL_VAUDP15	**Enables audio headphone speaker detection input mux** 00: Open 01: DACLP 10: DACLN 11: DACRP
6	RG_AUDTRIMBUF_EN_VAUDP15	**Enables audio offset trimming buffer**
5:4	RG_AUDTRIMBUF_GAINSEL_VAUDP15	**Selects audio offset trimming buffer gain** 00: 0dB 01: 6dB 10: 12dB 11: 18dB
3:0	RG_AUDTRIMBUF_INPUTMUXSEL_VAUDP15	**Selects audio offset trimming buffer mux** 0000: Open 0001: HPL 0010: HPR 0011: HSP 0100: HSN 0101: LOLP 0110: LOLN 0111: LORP 1000: LORN 1001: AVSS32 1010~1111: Unused

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1658 AUDDEC_ANA_CON9 AUDDEC Control Register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ABIDEC_RSVD0_VAUDP15								RG_ABIDEC_RSVD0_VA28							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_ABIDEC_RSVD0_VAUDP15	**Reserved one byte in VAUDP15 domain** [7]: Reserved [6:4]: HP Aux loop gain setting [3]: Enable HPR aux CMFB loop [2]: Enable HPL aux CMFB loop [1]: Enable HPR/L main CMFB loop [0]: Enable HP output stage turn-on timing control
7:0	RG_ABIDEC_RSVD0_VA28	**Reserved one byte in VA28 domain** [0]: Enable low-noise mode of DAC

165A AUDDEC_ANA_CON10 AUDDEC Control Register 10 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ABIDEC_RSVD2_VAUDP15								RG_ABIDEC_RSVD1_VAUDP15							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_ABIDEC_RSVD2_VAUDP15	Reserved one byte in VAUDP15 domain
7:0	RG_ABIDEC_RSVD1_VAUDP15	Reserved one byte in VAUDP15 domain

165C AUDDEC_ANA_CON11 AUDDEC Control Register 11 4900

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDBIASADJ_0_VAUDP15												RG_AUDZCDCLKSEL_VAUDP15	RG_AUDZCDMUXSEL_VAUDP15		
Type	RW												RW	RW		
Reset	0	1	0	0	1	0	0	1	0				0	0	0	0

Bit(s)	Name	Description
15:7	RG_AUDBIASADJ_0_VAUDP15	**Audio bias adjustment 0, bits:** [2:0] Headphone Left/Right DR bias current setting [5:3] Handset DR bias current setting. DR bias settings [8:6] Line-out DR bias current setting. DR bias settings 000: 4uA

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Bit(s)	Name	Description
		001: 5uA 010: 6uA 011: 7uA 100: 8uA 101: 9A 110: 10uA 111: 11uA
3	RG_AUDZCDCLKSEL_VAUDP15	**Increase ZCD comparator speed** 0: Normal speed 1: Improved speed
2:0	RG_AUDZCDMUXSEL_VAUDP15	**Selects zero crossing detection mux** 000: LOL 001: HPL and HPR 010: Handset 011: Unused 100: Bypass ZCD

165E **AUDDEC_ANA_CON12** **AUDDEC Control Register 12** **0155**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_AUDIBIASPWRDN_VAUDP15	RG_AUDBIASADJ_1_VAUDP15							
Type								RW	RW							
Reset								1	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
8	RG_AUDIBIASPWRDN_VAUDP15	**Power down control for IbiasDistrib circuit** 0: Enable 1: Disable
7:0	RG_AUDBIASADJ_1_VAUDP15	**Audio bias adjustment 1, bits:** [7:6] ZCD bias current setting 00: 3uA 01: 4uA 10: 5uA 11: 6uA [5:4] LOL/R ibias setting 00: 4uA 01: 5uA 10: 6uA 11: 7uA [3:2] HS ibias setting 00: 4uA 01: 5uA 10: 6uA 11: 7uA [1:0]: HPL/R ibias setting 00: 4uA 01: 5uA 10: 6uA 11: 7uA

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1660 **AUDDEC_ANA_CON13** **AUDDEC Control Register 13** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**RG_SEL_ENCODER_96K_VA28**	**RG_RSTB_ENCODER_VA28**	**RG_AUDGLB_PWRDN_VA28**		**RG_SEL_DELAY_VCORE**	**RG_SEL_DECODER_96K_VA28**	**RG_RSTB_DECODER_VA28**
Type										RW	RW	RW		RW	RW	RW
Reset										0	0	1		0	0	0

Bit(s)	Name	Description
6	RG_SEL_ENCODER_96K_VA28	**Selects audio ADC clock** 0: 3.25MHz 1: 6.5MHz
5	RG_RSTB_ENCODER_VA28	**Resets audio encoder** 0: Reset 1: Normal
4	RG_AUDGLB_PWRDN_VA28	**Power down control for audio global bias circuit** 0: Enable 1: Disable; default on
2	RG_SEL_DELAY_VCORE	**Selects AFIFO read clock delay** 0: 5ns 1: 10ns
1	RG_SEL_DECODER_96K_VA28	**Selects audio DAC clock** 0: 3.25MHz 1: 6.5MHz
0	RG_RSTB_DECODER_VA28	**Resets audio decoder** 0: Reset 1: Normal

1662 **AUDDEC_ANA_CON14** **AUDDEC Control Register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_LCLDO_VOSEL_VA18**	**RG_HCLDO_VOSEL_VA18**	**RG_VA28REFGEN_EN_VA28**	**RG_VA33REFGEN_EN_VA18**		**RG_LCLDO_ENC_REMOTE_SENSE_VA28**	**RG_LCLDO_ENC_PDDIS_EN_VA28**	**RG_LCLDO_ENC_EN_VA28**		**RG_LCLDO_REMOTE_SENSE_VA18**	**RG_LCLDO_PDDIS_EN_VA18**	**RG_LCLDO_EN_VA18**		**RG_HCLDO_REMOTE_SENSE_VA18**	**RG_HCLDO_PDDIS_EN_VA18**	**RG_HCLDO_EN_VA18**
Type	RW	RW	RW	RW		RW	RW	RW		RW	RW	RW		RW	RW	RW
Reset	0	0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
15	RG_LCLDO_VOSEL	**(Unused)**

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Bit(s)	Name	Description
	_VA18	
14	RG_HCLDO_VOSEL_VA18	**(Unused)**
13	RG_VA28REFGEN_EN_VA28	**Enables LCLDO_ENC Ref. gen.**
12	RG_VA33REFGEN_EN_VA18	**Enables HC_LDO, LC_LDO Ref. gen.**
10	RG_LCLDO_ENC_REMOTE_SENSE_VA28	**Selects LCLDO_ENC remote sense function** 0: Local sense 1: Remote sense
9	RG_LCLDO_ENC_PDDIS_EN_VA28	**Enables LCLDO_ENC power down discharge**
8	RG_LCLDO_ENC_EN_VA28	**Enable for LCLDO_ENC**
6	RG_LCLDO_REMOTE_SENSE_VA18	**Selects LCLDO remote sense function** 0: Local sense 1: Remote sense
5	RG_LCLDO_PDDIS_EN_VA18	**Enables LCLDO power down discharge**
4	RG_LCLDO_EN_VA18	**Enable for LCLDO**
2	RG_HCLDO_REMOTE_SENSE_VA18	**Selects HCLDO remote sense function** 0: Local sense 1: Remote sense
1	RG_HCLDO_PDDIS_EN_VA18	**Enables HCLDO power down discharge**
0	RG_HCLDO_EN_VA18	**Enable for HCLDO**

1664 **AUDDEC_ANA_CON15** **AUDDEC Control Register 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_AUDPMU_RSD0_VA28**				**RG_AUDPMU_RSD0_VA18**				**RG_AUDPMU_RSD0_VAUDP15**						**RG_NVREG_PULL0V_VAUDP15**	**RG_NVREG_EN_VAUDP15**
Type	RW				RW				RW						RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
15:12	RG_AUDPMU_RSD0_VA28	**Reserved in VA28/GND domain**
11:8	RG_AUDPMU_RSD0_VA18	**Reserved in VA18/GND domain**
7:4	RG_AUDPMU_RSD0_VAUDP15	**Reserved in VAUDP15/VAUDN18 domain**
1	RG_NVREG_PULL	0: DCC mode, switch is opened, NV output is -0.95V

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Bit(s)	Name	Description
	0V_VAUDP15	1: ACC mode, switch is closed, NV reg output is pulled to GND.
0	RG_NVREG_EN_VAUDP15	**Enable for NVREG**

1668 **AUDDEC_ELR_0** **AUDDEC ELR 0 Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_AUDHPTRIM_EN_VAUDP15	RG_AUDHPRFINETRIM_VAUDP15		RG_AUDHPLFINETRIM_VAUDP15		RG_AUDHPRTRIM_VAUDP15				RG_AUDHPLTRIM_VAUDP15			
Type				RW	RW		RW		RW				RW			
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12	RG_AUDHPTRIM_EN_VAUDP15	**Enable control of trim circuit of HP** 0: Disable trim circuit 1: Enable trim circuit
11:10	RG_AUDHPRFINETRIM_VAUDP15	**Fine-trims offset voltage of HPR** 01: -0.5mV 10: +0.5mV
9:8	RG_AUDHPLFINETRIM_VAUDP15	**Fine-trims offset voltage of HPL** 01: -0.5mV 10: +0.5mV
7:4	RG_AUDHPRTRIM_VAUDP15	**Trims offset voltage of HPR** 0000: 0V 0001: -0.5mV 0010: -1.5mV 0011: -2.5mV 0100: -3.5mV 0101: -4.5mV 0110: -5.5mV 0111: -6.5mV 1001: 0.5mV 1010: 1.5mV 1011: 2.5mV 1100: 3.5mV 1101: 4.5mV 1110: 5.5mV 1111: 6.5mV
3:0	RG_AUDHPLTRIM_VAUDP15	**Trims offset voltage of HPL** 0000: 0V 0001: -0.5mV 0010: -1.5mV 0011: -2.5mV 0100: -3.5mV 0101: -4.5mV 0110: -5.5mV 0111: -6.5mV 1001: 0.5mV 1010: 1.5mV

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Bit(s)	Name	Description
		1011: 2.5mV 1100: 3.5mV 1101: 4.5mV 1110: 5.5mV 1111: 6.5mV

1686 **ZCD_CON0** **ZCD Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_AUDZCDTIMEOUTMODESEL	RG_AUDZCDGAINSTEPSIZE		RG_AUDZCDGAINSTEPTIME			RG_AUDZCDENABLE
Type										RW	RW		RW			RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	RG_AUDZCDTIMEOUTMODESEL	**If no zero crossings are detected over a period of 30ms/5ms, a timeout will occur and the ZCD block enter SILENT mode** 0: 30ms 1: 5ms
5:4	RG_AUDZCDGAINSTEPSIZE	**Gain step size to change the internal gain of ZCD** 00: 1dB 01: 2dB 10: 4dB 11: 8dB
3:1	RG_AUDZCDGAINSTEPTIME	**Gain step time to change the internal gain of ZCD** 000: 0us 001: 250us 010: 500us 011: 1ms 100: 2ms 101: 4ms 110: 8ms 111: 16ms
0	RG_AUDZCDENABLE	**Enable for zero crossing detection (ZCD) function** 0: Disable 1: Enable

1688 **ZCD_CON1** **ZCD Control Register 1** **0F9F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDLORGAIN							RG_AUDLOLGAIN				
Type					RW							RW				
Reset					1	1	1	1	1			1	1	1	1	1

Bit(s)	Name	Description
11:7	RG_AUDLORGAIN	00000: +8dB 00001: +7dB 10010: -10dB

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Bit(s)	Name	Description
		11111: -40dB (mute)
4:0	RG_AUDLOLGAIN	00000: +8dB 00001: +7dB 10010: -10dB 11111: -40dB (mute)

168A ZCD_CON2 ZCD Control Register 2 0F9F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDHPRGAIN							RG_AUDHPLGAIN				
Type					RW							RW				
Reset					1	1	1	1	1			1	1	1	1	1

Bit(s)	Name	Description
11:7	RG_AUDHPRGAIN	00000: +8dB 00001: +7dB 10010: -10dB 11111: -40dB (mute)
4:0	RG_AUDHPLGAIN	00000: +8dB 00001: +7dB 10010: -10dB 11111: -40dB (mute)

168C ZCD_CON3 ZCD Control Register 3 001F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_AUDHSGAIN				
Type												RW				
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:0	RG_AUDHSGAIN	00000: +8dB 00001: +7dB 10010: -10dB 11111: -40dB (mute)

168E ZCD_CON4 ZCD Control Register 4 0707

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDIVRGAIN								RG_AUDIVLGAIN		
Type						RW								RW		
Reset						1	1	1						1	1	1

Bit(s)	Name	Description
10:8	RG_AUDIVRGAIN	000: +5dB 001: +4dB 010: +3dB 011: +2dB 100: +1dB

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Bit(s)	Name	Description
		101: 0dB 110: -1dB 111: -2dB
2:0	RG_AUDIVLGAIN	000: +5dB 001: +4dB 010: +3dB 011: +2dB 100: +1dB 101: 0dB 110: -1dB 111: -2dB

1690 **ZCD_CON5** **ZCD Control Register 5** **3F3F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDINTGAIN2								RG_AUDINTGAIN1					
Type			RO								RO					
Reset			1	1	1	1	1	1			1	1	1	1	1	1

Bit(s)	Name	Description
13:8	RG_AUDINTGAIN2	Monitor signal: Internal gain2
5:0	RG_AUDINTGAIN1	Monitor signal: Internal gain1

16C6 **ACCDET_CON0** **ACCDET Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AUDACCDETAUXADCSWCTRL_SEL											
Type					RW											
Reset					0											

Bit(s)	Name	Description
11	AUDACCDETAUXADCSWCTRL_SEL	**Controls the DA_NI_AUDACCDETAUXADCSWTROL signal is from SW or HW** 1'b0: HW mode 1'b1: SW mode

16C8 **ACCDET_CON1** **ACCDET Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										ACCDET_AN	ACCDET_EI	ACCDET_EI	ACCDET_EIN	ACCDET_EI	ACCDET_SE	ACCDET_EN

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16C8	ACCDET_CON1	ACCDET Control Register 1	0000

										ASW CTRL_SEL	NT1_SEQ_INIT	NT1_EN	T_SEQ_INIT	NT_EN	Q_INIT	
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	ACCDET_ANASWCTRL_SEL	**Selects who controls the connection between auxadc and accdet when in hook-key status** 1'b0: auxadc 1'b1: accdet
5	ACCDET_EINT1_SEQ_INIT	**Initializes EINT1 status default value** 1'b0: Disable 1'b1: Enable
4	ACCDET_EINT1_EN	**Enables EINT1 detection** 1'b0: Disable 1'b1: Enable
3	ACCDET_EINT_SEQ_INIT	**Initializes EINT status default value** 1'b0: Disable 1'b1: Enable
2	ACCDET_EINT_EN	**Enables EINT detection** 1'b0: Disable 1'b1: Enable
1	ACCDET_SEQ_INIT	**Initializes ACCDET status default value** 1'b0: normal mode 1'b1: initialized mode
0	ACCDET_EN	**Enables ACCDET** Must be set to 0 before switching to TV mode. 1'b0: Disable 1'b1: Enable

16CA	ACCDET_CON2	ACCDET Control Register 2	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												ACCDET_EINT1_PWM_EN	ACCDET_EINT_PWM_EN	ACCDET_MBIAS_PWM_EN	ACCDET_VTH_PWM_EN	ACCDET_CMP_PWM_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	ACCDET_EINT1_PWM_EN	**Enables PWM of ACCDET EINT1 unit** Disabled in TV mode. 1'b0: Disable 1'b1: Enable
3	ACCDET_EINT_PW	**Enables PWM of ACCDET EINT unit**

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Bit(s)	Name	Description
	M_EN	Disabled in TV mode. 1'b0: Disable 1'b1: Enable
2	ACCDET_MBIAS_PWM_EN	**Enables PWM of ACCDET MBIAS unit** Disabled in TV mode. 1'b0: Disable 1'b1: Enable
1	ACCDET_VTH_PWM_EN	**Enables PWM of ACCDET voltage threshold unit** Disabled in TV mode. 1'b0: Disable 1'b1: Enable
0	ACCDET_CMP_PWM_EN	**Enables PWM of ACCDET comparator** 1'b0: Disable 1'b1: Enable

16CC **ACCDET_CON3** **ACCDET Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_PWM_WIDTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_PWM_WIDTH	**ACCDET PWM width** PWM output frequency = 32,768/(PWM_WIDTH+1)Hz

16CE **ACCDET_CON4** **ACCDET Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_PWM_THRESH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_PWM_THRESH	**ACCDET PWM threshold** PWM output duty cycle = (PWM_THRESH+1)/(PWM_WIDTH+1) PWM output high time = (PWM_THRESH+1)/32,768 sec

16D0 **ACCDET_CON5** **ACCDET Control Register 5** **0101**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_FALL_DELAY	ACCDET_RISE_DELAY														

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16D0 **ACCDET_CON5** **ACCDET Control Register 5** **0101**

Type	RW	RW														
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15	ACCDET_FALL_DELAY	**Falling delay cycle compared to PWM waveform** To make sure the plug state is stable after ACCDET is disabled, the suitable falling delay cycle is necessary.
14:0	ACCDET_RISE_DELAY	**Rising delay cycle compared to PWM waveform** To make sure the plug state is stable before ACCDET is enabled, the suitable rising delay cycle is necessary.

16D2 **ACCDET_CON6** **ACCDET Control Register 6** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE0	**De-bounce time control of state 0** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock and 32,768Hz in the MIC mode.

16D4 **ACCDET_CON7** **ACCDET Control Register 7** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE1	**De-bounce time control of state 1** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock and 32,768Hz in the MIC mode.

16D6 **ACCDET_CON8** **ACCDET Control Register 8** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE2	**De-bounce time control of state 2** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock 32,768Hz in the MIC mode.

16D8 **ACCDET_CON9** **ACCDET Control Register 9** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE3	**De-bounce time control of state 3** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock 32,768Hz in the MIC mode.

16DA **ACCDET_CON10** **ACCDET Control Register 10** **0005**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE4	De-bounce time to control AUXADC when in state 0

16DE **ACCDET_CON12** **ACCDET Control Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_EINT1_IRQ_POLARITY	ACCDET_EINT_IRQ_POLARITY			ACCDET_EINT1_IRQ_CLR	ACCDET_EINT_IRQ_CLR		ACCDET_IRQ_CLR					ACCDET_EINT1_IRQ	ACCDET_EINT_IRQ		ACCDET_IRQ
Type	RW	RW			RW	RW		RW					RO	RO		RO
Reset	0	0			0	0		0					0	0		0

Bit(s)	Name	Description
15	ACCDET_EINT1_IRQ_POLARITY	**ACCDET EINT1 IRQ polarity** 1'b0: Falling edge 1'b1: Rising edge
14	ACCDET_EINT_IRQ_POLARITY	**ACCDET EINT IRQ polarity** 1'b0: falling edge

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Bit(s)	Name	Description
		1'b1: rising edge
11	ACCDET_EINT1_IRQ_CLR	**Clears ACCDET_EINT1 interrupt status** When ACCDET_EINT1 interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET_EINT design until both the interrupt status and IRQ_CLR are cleared.
10	ACCDET_EINT_IRQ_CLR	**Clears ACCDET_EINT interrupt status** When ACCDET_EINT interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET_EINT design until both the interrupt status and IRQ_CLR are cleared.
8	ACCDET_IRQ_CLR	**Clears ACCDET interrupt status** When ACCDET interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET design until both the interrupt status and IRQ_CLR are cleared.
3	ACCDET_EINT1_IRQ	**Clears ACCDET_EINT1 interrupt status**
2	ACCDET_EINT_IRQ	**Clear ACCDET_EINT interrupt status**
0	ACCDET_IRQ	**ACCDET interrupt status** Due to this register is cleared by the hardware, the interrupt edge-sensitive scheme should be adopted for this design.

16E2 ACCDET_CON14 ACCDET Control Register 14 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_AUDACCDETAUXADCSWCTRL	ACCDET_CMP_CLK	ACCDET_VTH_CLK	ACCDET_MBIAS_CLK												
Type	RO	RO	RO	RO												
Reset	0	0	0	0												

Bit(s)	Name	Description
15	DA_AUDACCDETAUXADCSWCTRL	ACCDET to AUXADC switch control
14	ACCDET_CMP_CLK	Comparator turn on control for accessory detection
13	ACCDET_VTH_CLK	Threshold voltage turn on for accessory detection
12	ACCDET_MBIAS_CLK	Earphone bias voltage turn on for accessory detection

16E4 ACCDET_CON15 ACCDET Control Register 15 0071

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ACCDET_EINT_PWM_WIDTH			ACCDET_EINT_PWM_THRESH				ACCDET_EINT_DEBOUNCE						

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16E4 ACCDET_CON15 ACCDET Control Register 15 0071

Type			RW			RW				RW						
Reset			0	0		0	0	0		1	1	1	0			

Bit(s)	Name	Description
13:12	ACCDET_EINT_PWM_WIDTH	**ACCDET EINT PWM width** 2'b00: 4ms 2'b01: 8ms 2'b10: 16ms 2'b11: 32ms
10:8	ACCDET_EINT_PWM_THRESH	**ACCDET EINT PWM threshold** 3'b000: 0.5ms 3'b001: 1ms 3'b010: 2ms 3'b011: 3ms 3'b100: 4ms 3'b101: 8ms 3'b110: 16ms 3'b111: 32ms
6:3	ACCDET_EINT_DEBOUNCE	**ACCDET EINT debounce time** 4'd0: 0ms (bypass) 4'd1: 0.12ms 4'd2: 0.25ms 4'd3: 0.5ms 4'd4: 0.75ms 4'd5: 1ms 4'd6: 2ms 4'd7: 4ms 4'd8: 8ms 4'd9: 16ms 4'd10: 32ms 4'd11: 48ms 4'd12: 64ms 4'd13: 128ms 4'd14: 256ms 4'd15: 512ms

16E6 ACCDET_CON16 ACCDET Control Register 16 0160

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_EINT_PWM_RISE_DELAY										ACCDET_EINT_PWM_FALL_DELAY					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	1	0	1	1					

Bit(s)	Name	Description
15:6	ACCDET_EINT_PWM_RISE_DELAY	**Rising delay cycle compared to PWM waveform** To make sure the plug state is stable before ACCDET_EINT is enabled, the

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Bit(s)	Name	Description
		suitable rising delay cycle is necessary.
5	ACCDET_EINT_PWM_FALL_DELAY	**Falling delay cycle compared to PWM waveform** To make sure the plug state is stable after ACCDET_EINT is disabled, the suitable falling delay cycle is necessary.

16EA ACCDET_CON18 ACCDET Control Register 18 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_NI_EINTCMPEN	AD_EINTCMPOUT														
Type	RO	RO														
Reset	0	0														

Bit(s)	Name	Description
15	DA_NI_EINTCMPEN	Monitor signal: DA_NI_EINTCMPEN
14	AD_EINTCMPOUT	Monitor signal : AD_EINTCMPOUT

16F0 ACCDET_CON21 ACCDET Control Register 21 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ACCDET_MON_FLAG_SEL											ACCDET_MON_FLAG_EN
Type					RW											RW
Reset					0	0	0	0	0	0	0	0				0

Bit(s)	Name	Description
11:4	ACCDET_MON_FLAG_SEL	Selects accdet monitor flag
0	ACCDET_MON_FLAG_EN	Enables accdet monitor flag

16F8 ACCDET_CON25 ACCDET Control Register 25 0071

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ACCDET_EINT1_PWM_WIDTH			ACCDET_EINT1_PWM_THRESH				ACCDET_EINT1_DEBOUNCE						
Type			RW			RW				RW						
Reset			0	0		0	0	0		1	1	1	0			

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Bit(s)	Name	Description
13:12	ACCDET_EINT1_PWM_WIDTH	**ACCDET EINT1 PWM width** 2'b00: 4ms 2'b01: 8ms 2'b10: 16ms 2'b11: 32ms
10:8	ACCDET_EINT1_PWM_THRESH	**ACCDET EINT1 PWM threshold** 3'b000: 0.5ms 3'b001: 1ms 3'b010: 2ms 3'b011: 3ms 3'b100: 4ms 3'b101: 8ms 3'b110: 16ms 3'b111: 32ms
6:3	ACCDET_EINT1_DEBOUNCE	**ACCDET EINT1 debounce time** 4'd0: 0ms (bypass) 4'd1: 0.12ms 4'd2: 0.25ms 4'd3: 0.5ms 4'd4: 0.75ms 4'd5: 1ms 4'd6: 2ms 4'd7: 4ms 4'd8: 8ms 4'd9: 16ms 4'd10: 32ms 4'd11: 48ms 4'd12: 64ms 4'd13: 128ms 4'd14: 256ms 4'd15: 512ms

16FA **ACCDET_CON26** **ACCDET Control Register 26** **0160**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_EINT1_PWM_RISE_DELAY										ACCDET_EINT1_PWM_FALL_DELAY					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	1	0	1	1					

Bit(s)	Name	Description
15:6	ACCDET_EINT1_PWM_RISE_DELAY	**Rising delay cycle compared to PWM waveform** To make sure the plug state is stable before ACCDET_EINT1 is enabled, the suitable rising delay cycle is necessary.
5	ACCDET_EINT1_PWM_FALL_DELAY	**Falling delay cycle compared to PWM waveform** To make sure the plug state is stable after ACCDET_EINT1 is disabled, the suitable falling delay cycle is necessary.

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16FC	ACCDET_CON27	ACCDET Control Register 27	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_NI_EINT1CMPEN	AD_EINT1CMPOUT														
Type	RO	RO														
Reset	0	0														

Bit(s)	Name	Description
15	DA_NI_EINT1CMPEN	Monitor signal: DA_NI_EINT1CMPEN
14	AD_EINT1CMPOUT	Monitor signal: AD_EINT1CMPOUT

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4 Application Notes

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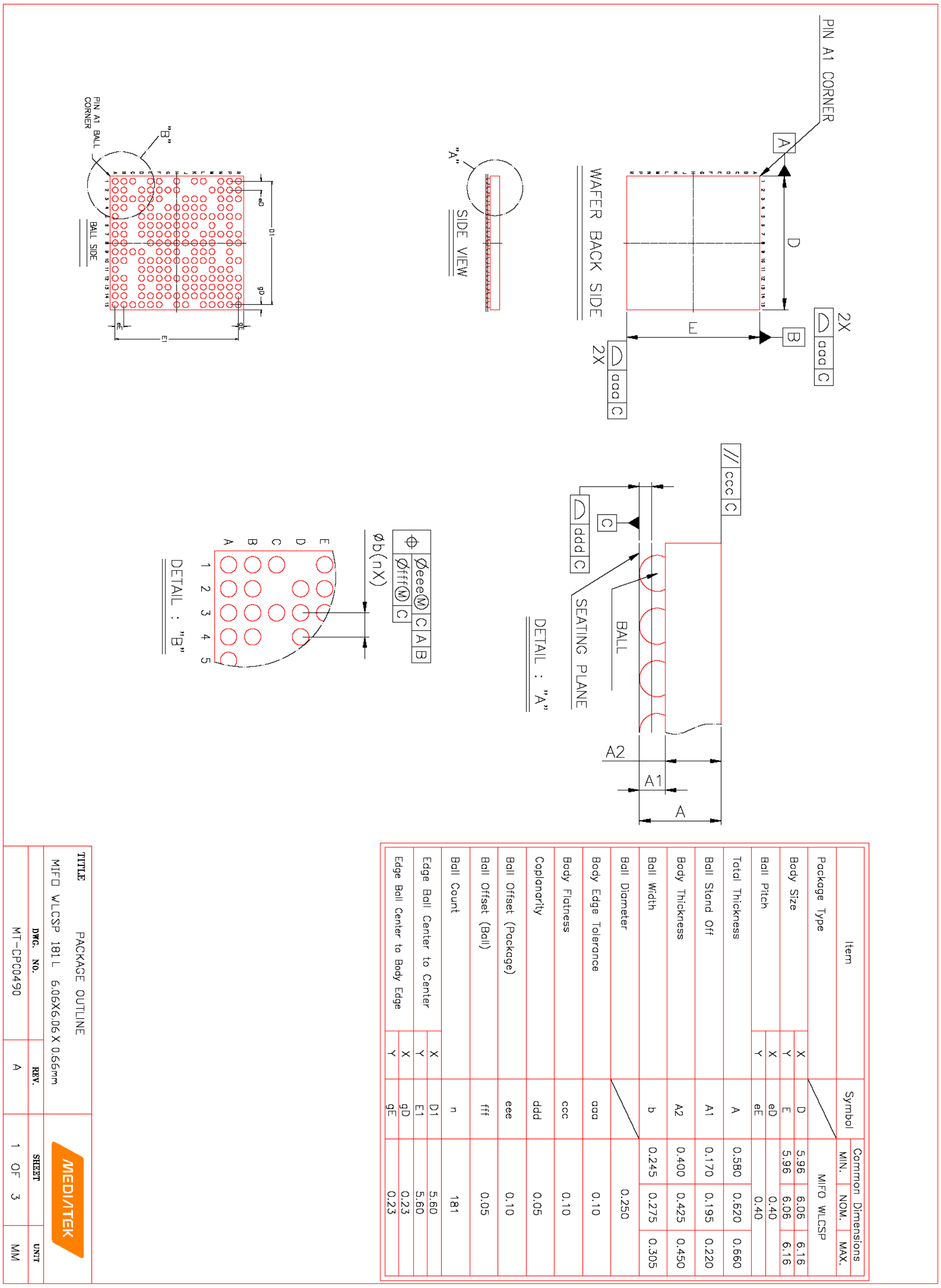
5 MT6356 Packaging

5.1 Package Dimensions



Item		Symbol	MIN.	NOM.	MAX.
Package Type				MIFO WLCSP	
Body Size	X	D	5.96	6.06	6.16
	Y	E	5.96	6.06	6.16
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Total Thickness		A	0.580	0.620	0.660
Ball Stand Off		A1	0.170	0.195	0.220
Body Thickness		A2	0.400	0.425	0.450
Ball Width		b	0.245	0.275	0.305
Ball Diameter				0.250	
Body Edge Tolerance		aaa		0.10	
Body Flatness		ccc		0.10	
Coplanarity		ddd		0.05	
Ball Offset (Package)		eee		0.10	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		181	
Edge Ball Center to Center	X	D1		5.60	
	Y	E1		5.60	
Edge Ball Center to Body Edge	X	gD		0.23	
	Y	gE		0.23	

Figure 5-1. Package dimension

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Appendix

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